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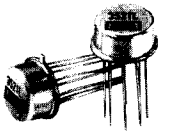


3521 SERIES
3522 SERIES

Ultra-Low Drift - FET Input OPERATIONAL AMPLIFIERS

FEATURES

- ULTRA-LOW DRIFT, 1μV/°C max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 1pA, max
- LOW NOISE
- HIGH COMMON-MODE REJECTION, 90dB, typ
- WIDE POWER SUPPLY RANGE, ±5VDC to ±20VDC

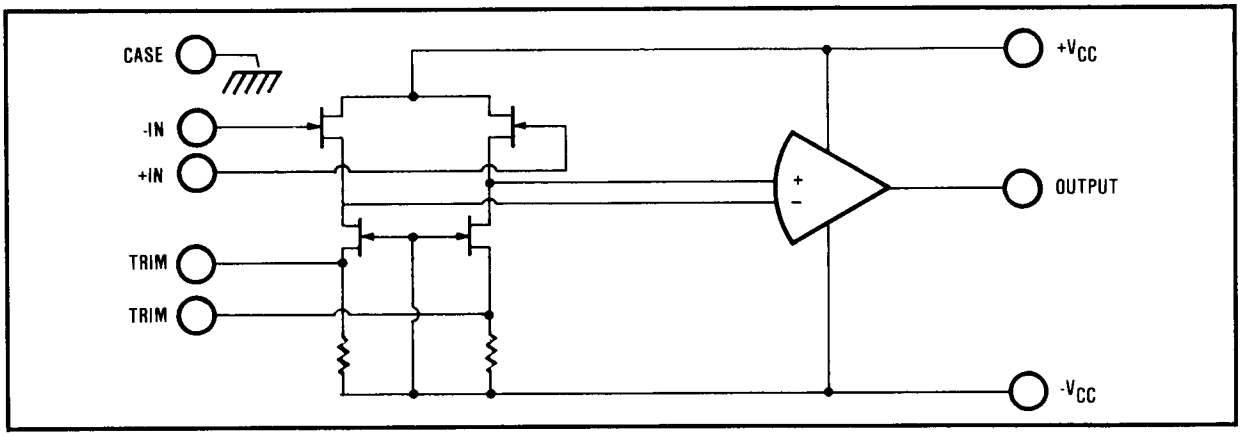
DESCRIPTION

With input offset voltage drifts as low as 1μV/°C, the Burr-Brown 3521 IC Operational Amplifier provides FET input performance combined with drift equal to the best bipolar IC's (e.g., BB3500E). The spectacular performance is achieved through truly state-of-the-art hybrid design and manufacturing, including monolithic FET pairs and active laser-trimming.

The 3521 and 3522 have an exceptionally fast thermal response. This fast warm-up is achieved without any heat-sinking.

While low drift and FET input impedance are the outstanding features of the 3521 and 3522 other specifications have not been compromised. They are internally compensated for unity-gain configuration and the initial voltage offset is guaranteed less than 250μV so for most applications the 3521 is ready to "plug-in and go." Like other low drift IC's from Burr-Brown the 3521 and 3522 have ample speed and bandwidth for most any application. (Slew rate = 0.6V/μsec). The high common-mode rejection ratio (90dB, typ.) enables them to be used as a 0.01% accurate buffer with low drift and extremely-high input impedance. The 3521/3522 also have very-low input noise to complement the low drift. The output is current limited to provide protection for continuous output shorts to common.

The 3521/3522 are pin-compatible with 741-type amplifiers, but provide FET input performance with ultra-low drift while exceeding all other specifications for general purpose operational amplifiers of the 741-type. Burr-Brown tests and guarantees all units to meet all max/min specifications.



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SPECIFICATIONS

ELECTRICAL

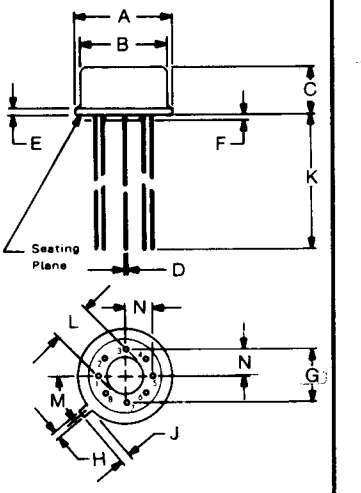
Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3521H	3521J	3521K	3521L	3521R
OPEN-LOOP GAIN, DC					
Rated Load, min	94dB	*	*	*	*
RATED OUTPUT					
Voltage, min	+10V	*	*	*	*
Current, min	±10mA	*	*	*	*
Output Impedance	100Ω	*	*	*	*
FREQUENCY RESPONSE					
Unity Gain, Open-Loop	1.5MHz	*	*	*	*
Full Power Response, min	10kHz	*	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*	*
INPUT OFFSET VOLTAGE					
Initial Offset, 25°C, max	±500μV	250μV	250μV	250μV	250μV
vs Temp (0°C to +70°C), **max	±10μV/°C	±5μV/°C	2μV/°C	±1μV/°C	±5μV/°C
vs Temp (-25°C to +85°C)	±15μV/°C	±8μV/°C	±4μV/°C	±2μV/°C	±2μV/°C
vs Supply Voltage	±25μV/V	*	*	*	*
vs Time	5μV/mo	*	*	*	*
INPUT BIAS CURRENT					
Initial Bias, 25°C, max	-20pA	*	-15pA	-10pA	*
(doubles every +10°C)					
vs Supply Voltage	1pA/V	*	*	*	*
INPUT DIFFERENCE CURRENT					
Initial difference, 25°C	±2pA	*	*	*	*
INPUT IMPEDANCE					
Differential	$10^{11}\Omega$	*	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*	*
INPUT NOISE					
Voltage, 0.01Hz - 10Hz, p-p	4μV	*	*	*	*
Voltage, 10Hz - 1kHz, rms	2μV	*	*	*	*
Current, 0.01Hz - 10Hz, p-p	0.3pA	*	*	*	*
Current, 10Hz - 1kHz, rms	0.6pA	*	*	*	*
INPUT VOLTAGE RANGE					
Common-mode Voltage	±10V	*	*	*	*
Common-mode Rejection	90dB	*	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*	*
POWER SUPPLY					
Rated Voltage	±15VDC	*	*	*	*
Voltage Range, derated	±5 to ±20VDC	*	*	*	*
Current, quiescent	±4mA	*	*	*	*
TEMPERATURE RANGE					
Specification	0°C to +70°C	*	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*	*

*Specification same as for 3521H.
**-55°C to +125°C for 3521R.

MECHANICAL

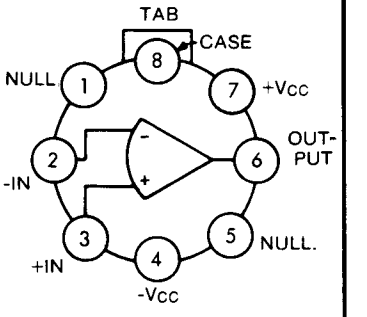
(TO-99 PACKAGE)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

(TOP VIEW)



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3521/3522. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3521. Note that the offset voltage has stabilized in less than 4 minutes. Similar warm-up times for some discrete low drift operational amplifiers range from 7 to 15 minutes.

Offset voltage response to thermal shock can provide some real suprises, particularly for amplifiers packaged in discrete modules. Again the TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3521/3522 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

BIAS CURRENT EFFECTS

The low bias currents and offset currents of FET input stages overcome most of the source resistance limitations of bipolar operational amplifiers. However, for very large source resistances or large unbalances in source resistance (5MΩ and up) the input offset voltage and drift will be affected as shown in Figures 3 and 4.

COMMON-MODE PROPERTIES

The input stage of the 3521 is a monolithic FET pair, which affords very good matching between the two input transistors. This close matching makes the 90dB common-mode rejection ratio (CMRR) possible. Because of its excellent common-mode properties the 3521 may be used as a 0.01% accurate buffer amplifier for inputs between ±10V. Figure 5 below illustrates typical common-mode performance of the 3521.

POWER SUPPLIES AND DRIFTS

Note that a power supply change of 40mV will typically introduce an input offset voltage change of 1μV. Since power supply drift will have the same effect as offset voltage drift, the power supply temperature coefficients of ±15V supplies should be about 0.1%/°C for optimum drift performance of the 3521L.

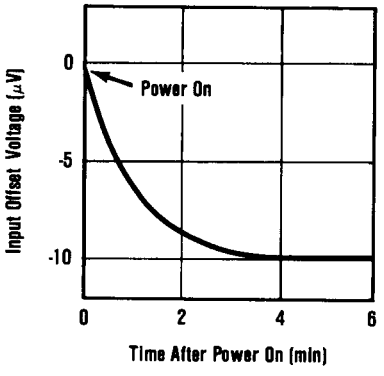


FIGURE 1. Typical Warm-up Drift.

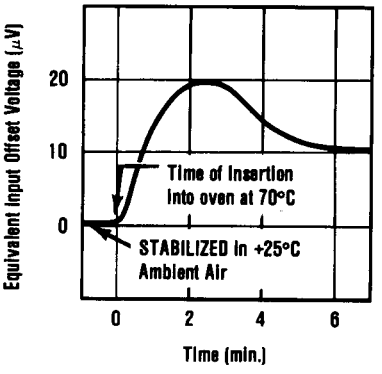
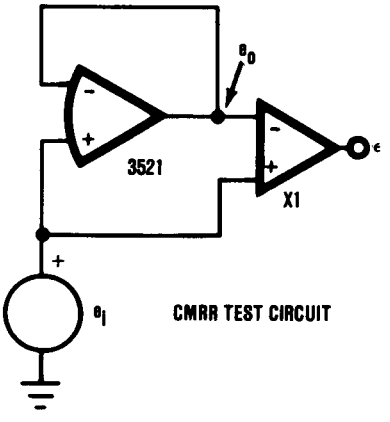


FIGURE 2. Effect of Thermal Shock on Offset Voltage.



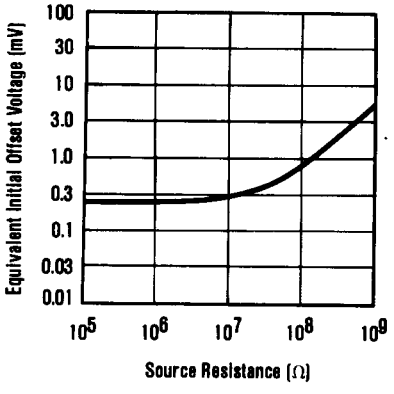


FIGURE 3. Typical Effects of Source Resistance on Initial Offset Voltage.

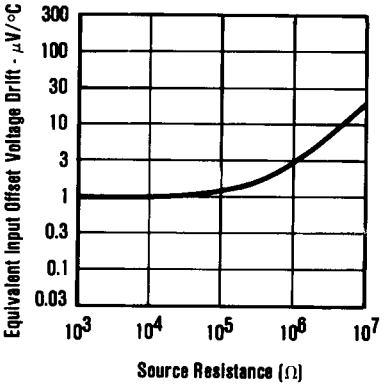


FIGURE 4. Typical Effects of Source Resistance on Equivalent Input Offset Voltage Drift.

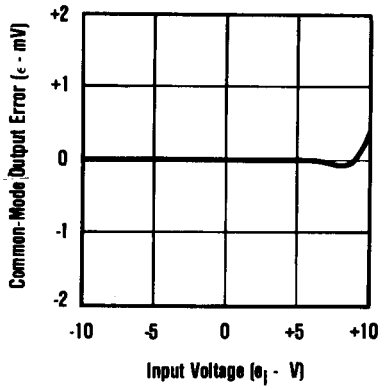
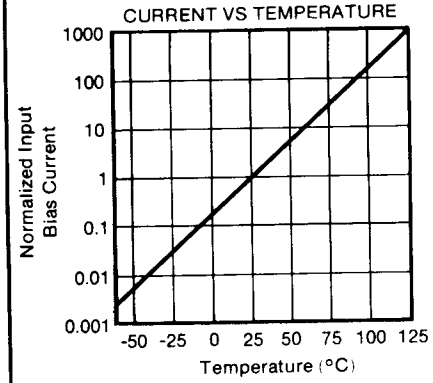


FIGURE 5. Common-Mode Performance.

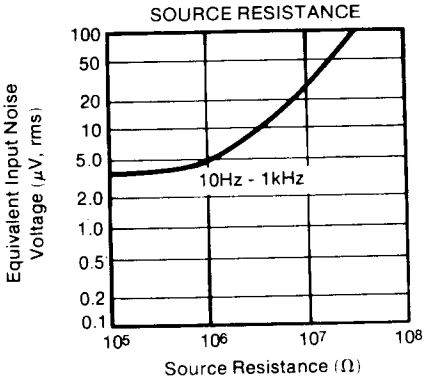
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC unless otherwise specified)

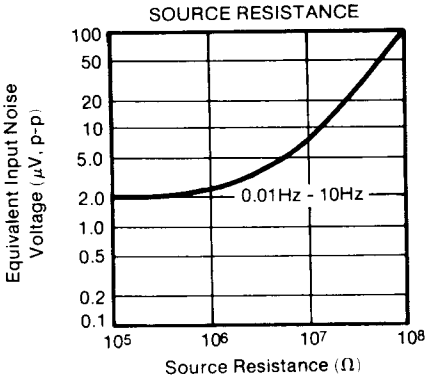
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



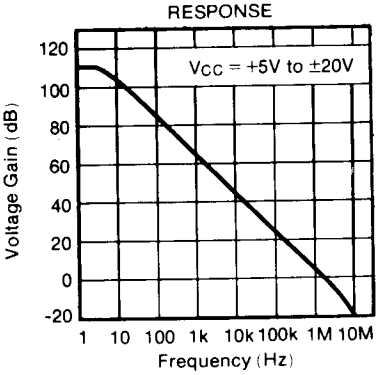
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



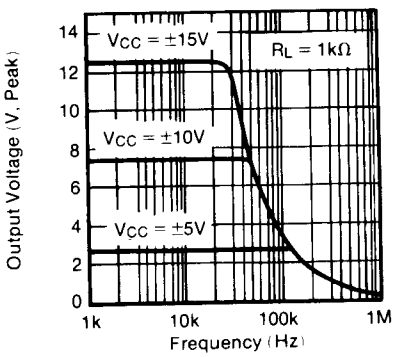
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



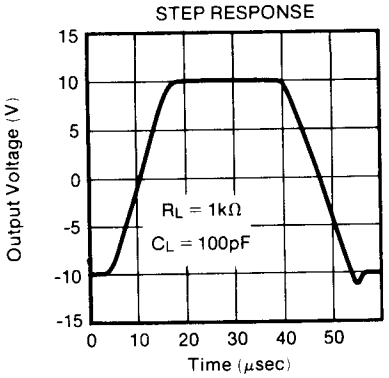
OPEN-LOOP FREQUENCY RESPONSE



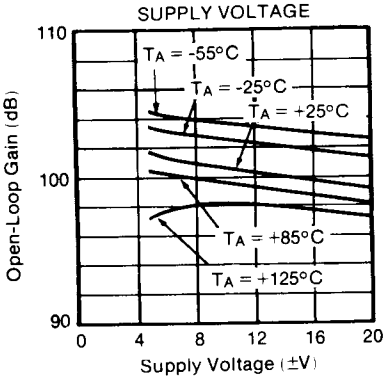
OUTPUT VOLTAGE VS FREQUENCY



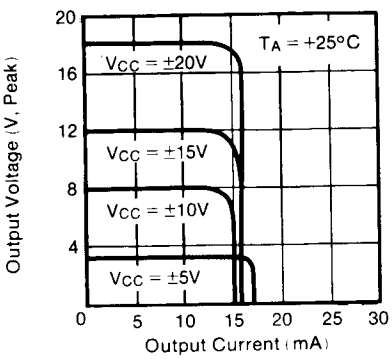
VOLTAGE FOLLOWER STEP RESPONSE



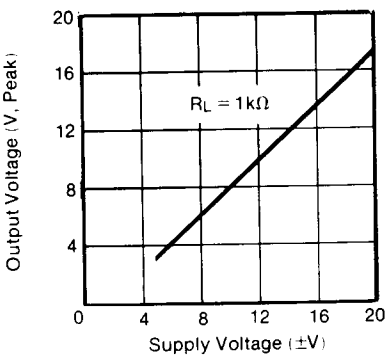
VOLTAGE GAIN VS SUPPLY VOLTAGE



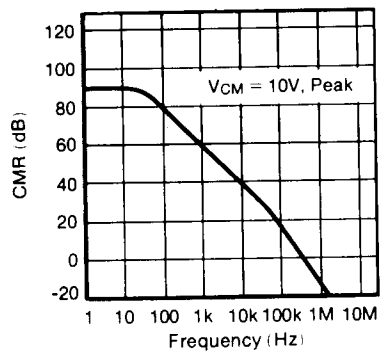
OUTPUT VOLTAGE VS OUTPUT CURRENT



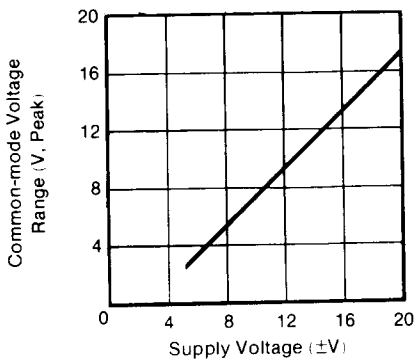
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



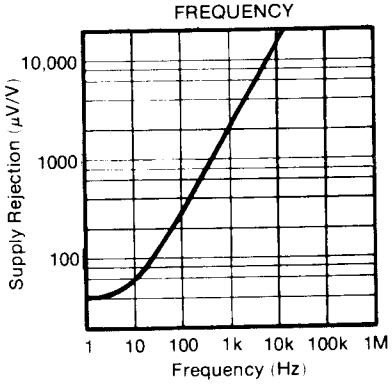
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



ELECTRICAL (CONT)

Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3522J	3522K	3522L	3522S
OPEN-LOOP GAIN, DC				
Rated Load, min	94dB	*	*	*
RATED OUTPUT				
Voltage, min	±10V	*	*	*
Current, min	±10mA	*	*	*
Output Impedance	100Ω	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Open-loop	1MHz	*	*	*
Full Power Response, min	10kHz	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, 25°C, max	±1mV	±500μV	±500μV	±500μV
vs Temp (0°C to +70°C), max	±50μV/°C	±10μV/°C	±10μV/°C	
(-55°C to +125°C), max				±25μV/°C
vs Supply Voltage	±25μV/mo	*	*	*
vs Time	±10μV/mo	*	*	*
INPUT BIAS CURRENT**				
Input Bias, 25°C, max	-10pA	-5pA	-1pA	-5pA
(doubles every +10°C)				
vs Supply Voltage	±0.1pA/V	*	*	*
INPUT DIFFERENCE CURRENT				
Initial Difference, +25°C	±2pA	±1pA	±0.5pA	±1pA
INPUT IMPEDANCE				
Differential	$10^{11}\Omega$	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	4μV	*	*	*
Voltage, 10Hz to 1kHz, rms	2μV	*	*	*
Current, 0.01Hz to 10Hz, p-p	0.3pA	*	*	*
Current, 10Hz to 1kHz, rms	0.6pA	*	*	*
INPUT VOLTAGE RANGE				
Common-mode Voltage	±10V	*	*	*
Common-mode Rejection	90dB	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*
POWER SUPPLY				
Rated Voltage	±15VDC	*	*	*
Voltage Range, derated	±5VDC to ±20VDC	*	*	*
Current, quiescent	±4mA	*	*	*
TEMPERATURE RANGE				
Specification	0°C to +70°C	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

*Specification same as for 3522J.
**After Warm-Up.

WIRING CONSIDERATIONS (Shielding and Guarding)

The ultra-low drift, very-low bias current and high input impedance make the 3521/3522 well suited to a number of unique applications. However, careless signal wiring can degrade "system" performance several orders of magnitude below the 3521/3522 capability.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large value feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the units. Perhaps more important, unbalanced leakage paths (when is leakage ever balanced?) can generate significant input offset voltages when large source impedances (100kΩ and up) are involved. To avoid leakage problems, it is recommended that the inputs of the 3521 be wired to teflon standoffs. If the unit must be soldered directly into a printed circuit board, utmost care should be used in designing the board layout. A "guard" pattern should completely surround the two input leads and be connected to a low impedance point at the common-mode input voltage. Figure 6 shows suggested guard connections for various amplifier feedback configurations. The amplifier case should be connected to any input shield or guard via pin 8.

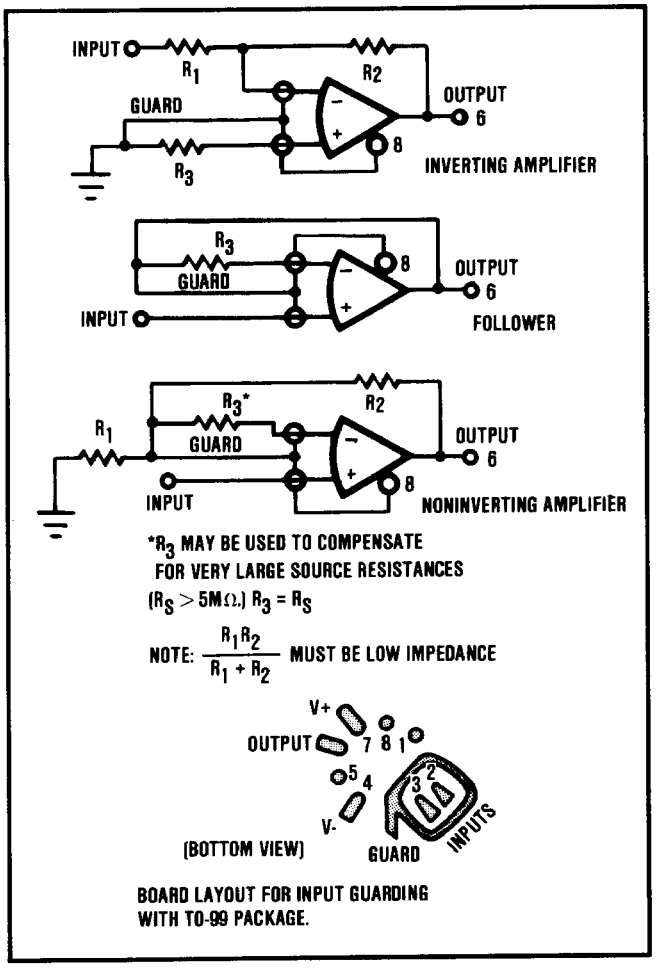


FIGURE 6. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

The 3521 has a low initial offset (250μV) compatible with its low drift. However, some high accuracy applications may require external nulling of even this small initial offset voltage. Virtually any offset voltage adjustment method can increase offset voltage drift unless some care is used. For example, the initial offset voltage of most monolithic op amps (BB 3500, 741-types, 101, etc.) may be nulled using a single potentiometer, but offset voltage drift is typically increased by about 3μV/°C for each mV of offset voltage adjust. This same relationship will also hold for the 3521.

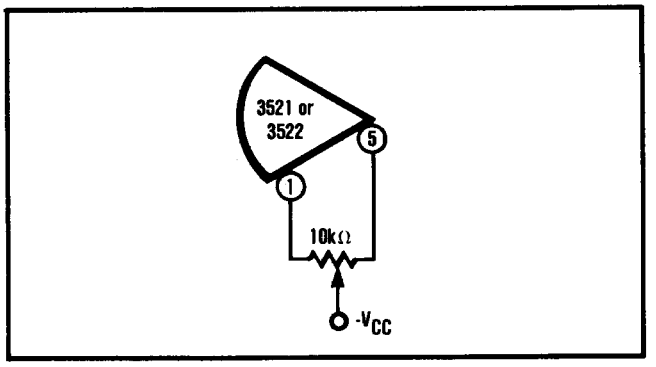


FIGURE 7. Single Potentiometer Adjust at Op Amp Trim Terminals.

Advantages:

1. Simplest circuit.
2. Compatible with most IC op amps.

Disadvantages:

1. Drift increased by circuit about 0.75μV/°C for 3521.

TEMPERATURE COMPENSATED POTENTIOMETER OFFSET VOLTAGE ADJUST

If the circuit in Figure 7 is replaced with a circuit which "drifts" with temperature, nulling the offset voltage will not increase the drift by so large an amount. The circuit shown in Figure 8 may be used to null initial offset voltage and drift will increase only about 0.5μV/°C for each mV of offset adjust. In the case of the 3521, this zeroing circuit will typically add at most 0.14μV/°C.

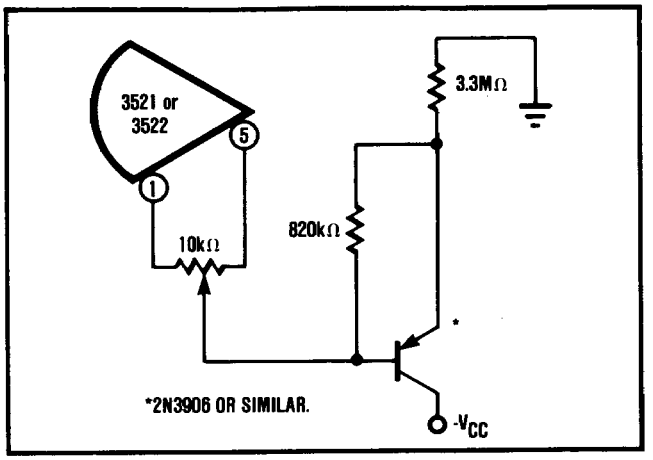


FIGURE 8. Temperature Compensated Potentiometer Null.