MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC12012

5-2 ORIG

003406

T-3406 mcT

MECL PLL COMPONENTS

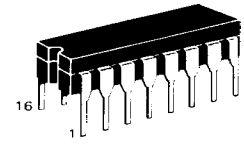
TWO-MODULUS PRESCALER

TWO-MODULUS PRESCALER

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide-by-5/divide-by-6 prescaler; 2) a divide-by-2 prescaler, and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide-by-N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

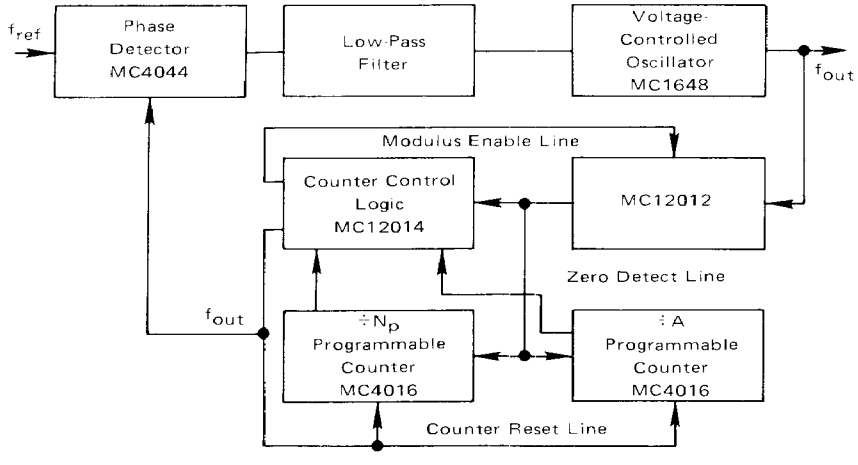
- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or −5.2 V Operation*
- 200 MHz (Typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using −5.2 supply, ground pin 16 (V_{CC}) and apply −5.2 V to pin 8 (V_{EE}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



PIN ASSIGNMENT

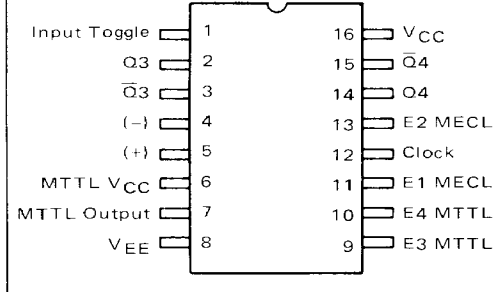
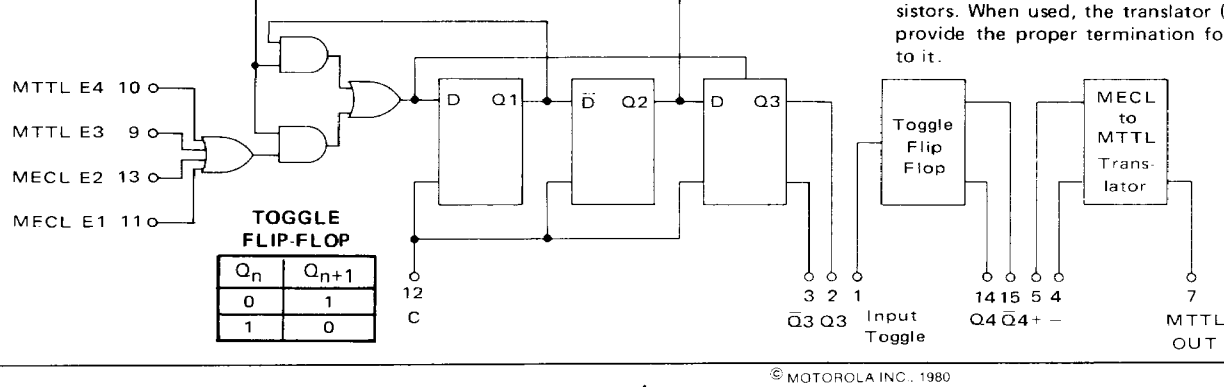


FIGURE 2 – LOGIC DIAGRAM



TOGGLE FLIP-FLOP

Q_n	Q_{n+1}
0	1
1	0

To obtain an MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively. The MECL outputs (2, 3, 14, 15) require terminating resistors. When used, the translator (4 and 5) will provide the proper termination for connection to it.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current Continuous Surge	I_O	 50 100	mAdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
(Recommended Maximum Ratings above which performance may be degraded)			
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L (mA)	I_{OL} (mA)	I_{OH} (mA)
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	+0.3	-3.2	4.4	-5.2	2.5	16	1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	+0.3	-3.2	-4.4	-5.2	2.5	16	1.6
75°C	-0.720	-1.830	-1.045	-1.450	-4.7	+0.3	-3.2	4.4	-5.2	2.5	16	1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	V_{CC} Gnd
Power Supply Drain Current	I_E	8		140	–	130	–	140	mAdc									8				6,16
Input Current	I_{INH1}	12		200	–	200	–	200	µAdc	12		–						8				16
	I_{INH2}	1 11 13	– –	100 ↓	– –	100 ↓	– –	100 ↓	µAdc	1 11 13	– –							8 8 8				16 16 16
	I_{INH3}	9 10	– –	40 40	– –	40 40	– –	40 40	µAdc			– –			9 10			8 8				16 16
	I_{INH4}	4 5	4.0 4.0	6.5 6.5	4.0 4.0	6.5 6.5	4.0 4.0	6.5 6.5	mAdc mAdc	5 5	4 4	–						8 8				9 6
Leakage Current	I_{INL1}	1 11 12 13	-3.0 ↓	– ↓	-2.0 ↓	– ↓	-3.0 ↓	– ↓	µAdc ↓	– – – –	– – – –							1,8 8,11 8,12 8,13				16 ↓
	I_{INL2}	9 10	-1.1 -1.1	-2.5 -2.5	-1.1 -1.1	-2.5 -2.5	-1.1 -1.1	-2.5 -2.5	mAdc mAdc	–	–	–		9 10				8 8				16 16
	I_{INL3}	4 5	4.0 3.0	7.0 5.0	4.0 3.0	7.0 5.0	4.0 3.0	7.0 5.0	mAdc mAdc	4 4	5 5	–						8 8				16 16
Logic "1" Output Voltage ②	V_{OH1}	2 3 14 15	-1.000 ↓	-0.840 ↓	-0.960 ↓	-0.810 ↓	-0.900 ↓	-0.720 ↓	Vdc ↓	– – – –	11,13 11,13 – –	– –		9,10 9,10	–			8 ↓	2 3 14 15	–		16 ↓
	V_{OH2}	7	-2.800	–	-2.800	–	-2.800	–	Vdc	5	4	–						8			7	6
Logic "0" Output Voltage ②	V_{OL1}	2 3 14 15	-1.870 ↓	-1.635 ↓	-1.850 ↓	-1.620 ↓	-1.830 ↓	-1.595 ↓	Vdc ↓	– – – –	11,13 11,13 – –	– –		9,10 9,10	–			8 ↓	2 3 14 15	–	–	16 ↓
	V_{OL2}	7	–	-4.700	–	-4.700	–	-4.700	Vdc	4	5	–						8			7	6
Logic "1" Threshold Voltage	V_{OHA}	2 ③ 3 ③ 14 ④ 15 ④	-1.020 ↓	– – – –	-0.980 ↓	– – – –	-0.920 ↓	– – – –	Vdc ↓	– – – –	– – – –	11,13 11,13 –				9,10 9,10		8 ↓	2 3 14 15			16 ↓
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤ 3 ⑤ 14 ④ 15 ④	– – – –	-1.615 ↓	– – – –	-1.600 ↓	– – – –	-1.575 ↓	Vdc ↓	– – – –	– – – –	– –	11,13 11,13 –	– – – –	–		9,10 9,10	8 ↓	2 3 14 15			16 ↓
Short Circuit Current	I_{OS}	7	-20	-65	-20	-65	-20	-65	mAdc	5	4	–						8			–	6

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts)								
	V_{IHmax}	$V_{IL min}$	V_{IHAmax}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IH}	V_{ILH}	V_{CC}
0°C	-4.160	-3.180	-3.855	-3.560	+0.5	+5.5	0	-0.5	5
25°C	-4.190	-3.200	-3.895	-3.575	+0.5	+5.5	0	-0.5	5
75°C	-4.280	-3.220	-3.955	-3.600	+0.5	+5.5	0	-0.5	5

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IH}	V_{ILH}	V_{CC}
Power Supply Drain Current	I_E	8	–	135	–	125	–	135	mAdc									6,16
Input Current	I_{INH1}	12	–	200	–	200	–	200	µAdc	12								16
	I_{INH2}	1	–	100	–	100	–	100	µAdc	1								16
		11		↓		100		↓		11								16
		13				100				13								16
	I_{INH3}	9	–	40	–	40	–	40	µAdc	–					9			16
		10	–	40	–	40	–	40		–					10			16
	I_{INH4}	4	4.0	6.5	4.0	6.5	4.0	6.5	mAdc	5	4							6
		5	4.0	6.5	4.0	6.5	4.0	6.5	mAdc	5	4							6
Leakage Current	I_{INL1}	1	-3.0		2.0		-3.0	–	µAdc	–								16
		11	↓		↓		↓	–		–								↓
		12						–		–								
		13						–		–								
	I_{INL2}	9	-2.5	-1.1	-2.5	-1.1	-2.5	-1.1	mAdc	–	–			9				16
		10	-2.5	-1.1	-2.5	-1.1	-2.5	-1.1	mAdc	–	–			10				16
	I_{INL3}	4	4.0	7.0	4.0	7.0	4.0	7.0	mAdc	4	5							6
		5	3.0	5.0	3.0	5.0	3.0	5.0	mAdc	4	5							6
Logic "1" Output Voltage ②	V_{OH1}	2	4.000	4.160	4.040	4.190	4.100	4.280	Vdc	–	11,13			9,10				16
		3	↓	↓	↓	↓	↓	↓		–	11,13			9,10				↓
		14								–	–							
		15								–	–							
	V_{OH2}	7	2.400	–	2.400	–	2.400	–	Vdc	5	4							6
Logic "0" Output Voltage ②	V_{OL1}	2	3.180	3.415	3.200	3.430	3.220	3.455	Vdc	–	11,13			9,10				16
		3	↓	↓	↓	↓	↓	↓		–	11,13			9,10				↓
		14								–	–							
		15								–	–							
	V_{OL2}	7	–	0.500	–	0.500	–	0.500	Vdc	4	5							6
Logic "1" Threshold Voltage	V_{OHA}	2 ③	3.980		4.020	–	4.080	–	Vdc	–		11,13				9,10		16
		3 ③	↓		↓	–	↓	–		–		11,13				9,10		↓
		14 ④				–		–		–								
		15 ④				–		–		–								
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	3.435	–	3.450	–	3.475	Vdc	–	–	–	11,13				9,10	16
		3 ⑤		↓		↓		↓		–	–	–	11,13				9,10	↓
		14 ④			–		–			–	–	–						
		15 ④								–	–	–						
Short Circuit Current	I_{OS}	7	-20	-65	-20	-65	-20	-65	mAdc	5	4							6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} +1.100	V_{ILmin} +0.130	V_F -3.0 V	V_{EE} 3.0 or 3.2	V_{CC} +2.0
Propagation Delay (See Figures 3 and 4)	t_{12+2+}	12,2	–	–	–	3.0	4.0	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{12+3+}	12,3	–	–	–	3.0	↓	–	–	↓	↓	–	–	–	11,13	9,10	↓	↓
	t_{12+}	12,2	–	–	–	2.8	–	–	–	–	–	–	–	–	11,13	9,10	–	–
	t_{12+3-}	12,3	–	–	–	2.8	–	–	–	–	–	–	–	–	11,13	9,10	–	–
	t_{1+14+}	1,14	–	–	–	3.0	–	–	–	–	1	–	–	–	–	–	–	–
	t_{1+15+}	1,15	–	–	–	3.0	–	–	–	–	↓	–	–	–	–	–	–	–
	t_{1+14-}	1,14	–	–	–	2.8	–	–	–	–	↓	–	–	–	–	–	–	–
	t_{1+15-}	1,15	–	–	–	2.8	↓	–	–	–	↓	–	–	–	–	–	–	–
	t_{5+7+}	5,7	–	–	–	8.0	12.0	–	–	–	A	–	–	–	–	–	↓	↓
	t_{5-7-}	5,7	–	–	–	5.0	10.0	–	–	↓	A	–	–	–	–	–	–	–
Output Rise Time (See Figure 4)	t_{2+}	2	–	–	–	–	3.0	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3+}	3	–	–	–	–	↓	–	–	↓	12	–	–	–	11,13	9,10	↓	↓
	t_{14+}	14	–	–	–	–	–	–	–	–	1	–	–	–	–	–	–	–
	t_{15+}	15	–	–	–	–	↓	–	–	↓	1	–	–	–	–	–	↓	↓
Output Fall Time (See Figure 4)	t_{2-}	2	–	–	–	–	2.5	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3-}	3	–	–	–	–	↓	–	–	↓	12	–	–	–	11,13	9,10	↓	↓
	t_{14-}	14	–	–	–	–	–	–	–	–	1	–	–	–	–	–	–	–
	t_{15-}	15	–	–	–	–	↓	–	–	↓	1	–	–	–	–	–	↓	↓
Setup Time (See Figure 5)	t_{setup1}	11,13	–	4.0	–	2.4	3.0	–	4.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{setup2}	9,10	–	7.0	–	5.0	7.0	–	8.5	ns	12	–	9/10	–	11,13	10/9	8	6,16
Release Time (See Figure 5)	t_{rel1}	11,13	–	2.5	–	1.2	2.0	–	2.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{rel2}	9,10	–	4.0	–	2.5	3.5	–	2.0	ns	12	–	9/10	–	11,13	10/9	8	6,16
Toggle Frequency	f_{max}									MHz								
Figure 6 (÷5)	↓	2	–	–	175	200	–	–	–	↓	–	–	–	11	13	9,10	8	16
(÷6)		2	–	–	↓	↓	–	–	–		–	–	–	–	11,13	9,10	↓	↓
(÷2)		14	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–
Figure 7 (÷10 or 11)		14	–	–			–		–		–							

① All MECL outputs (2, 3, 14, 15) are terminated to V_{EE} through an external 510 Ω resistor during the DC tests.

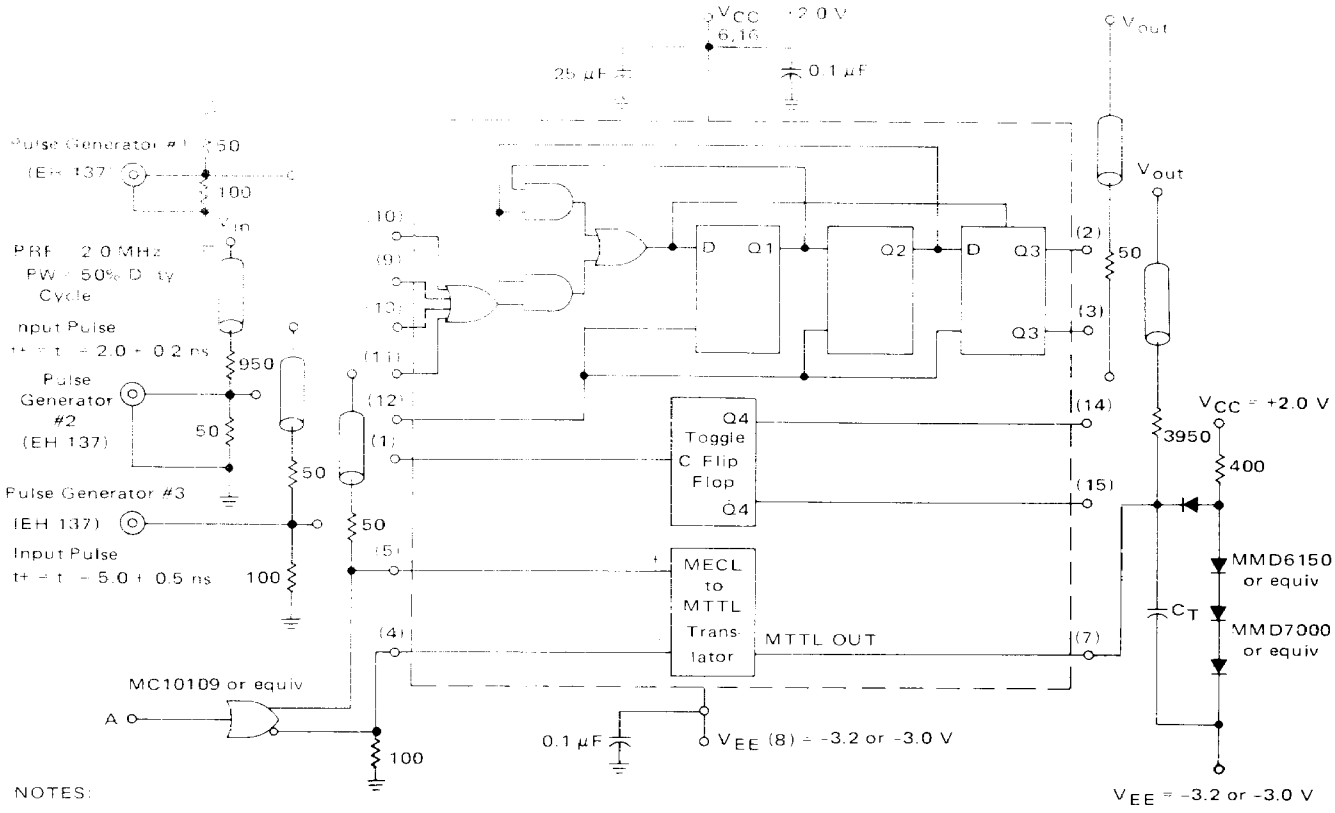
② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is

③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is

④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of

⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

FIGURE 3 — AC TEST CIRCUIT



NOTES:

All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

All unused cables must be terminated with 50 ohms.

All resistors are ± 1%.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe.

The 50-ohm resistor and the scope termination impedance constitute a 2:1 attenuator probe.

FIGURE 4 — AC VOLTAGE WAVEFORMS

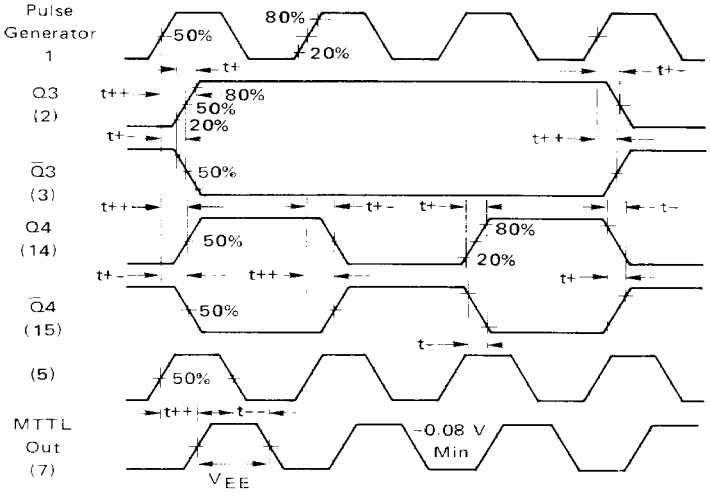


FIGURE 5 – SETUP AND RELEASE TIME WAVEFORMS

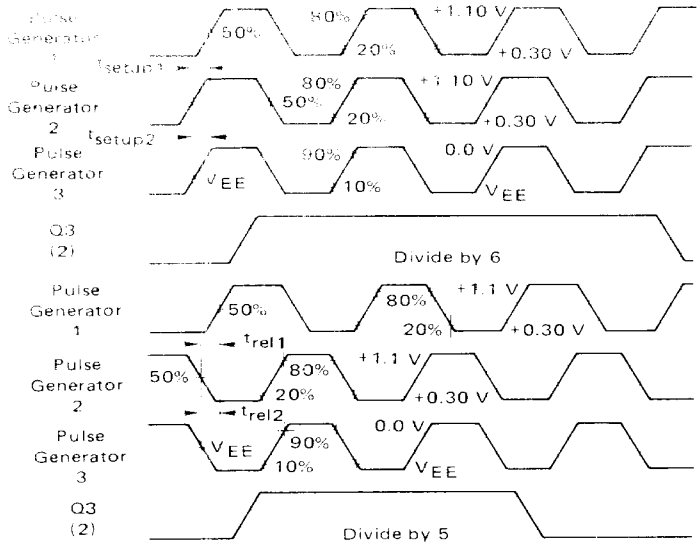
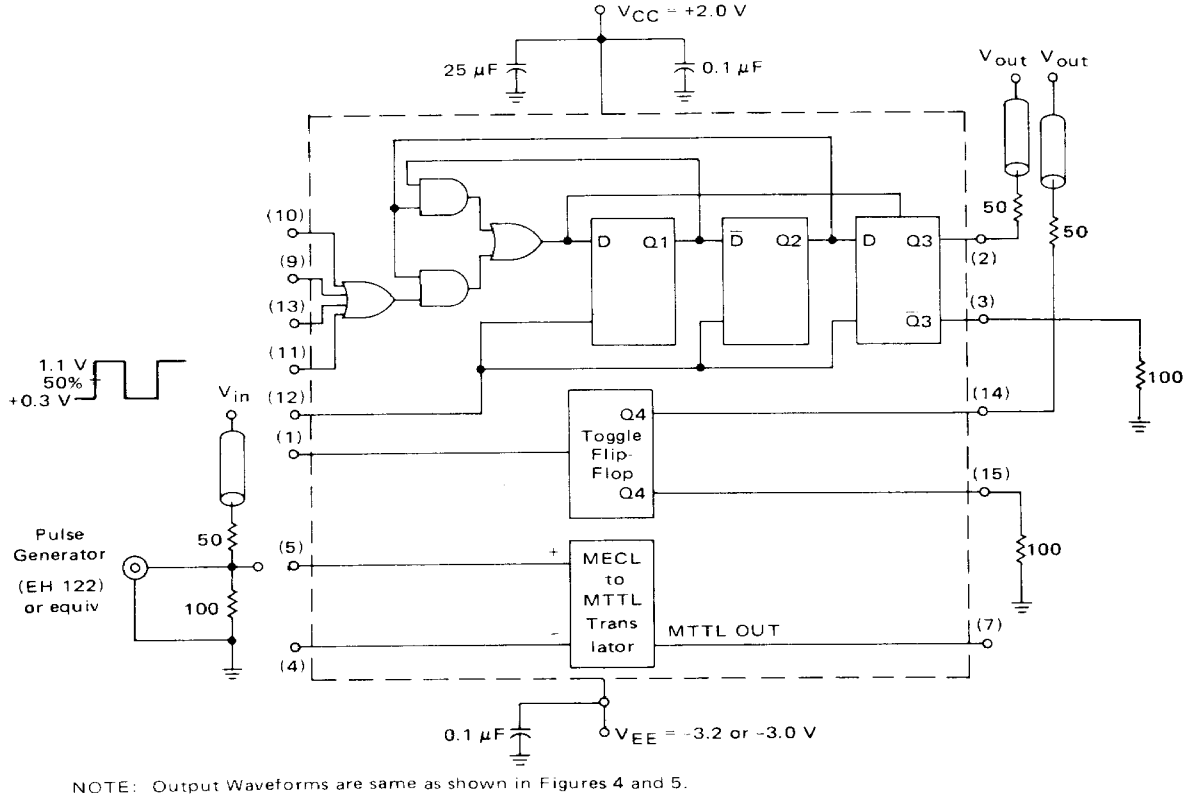
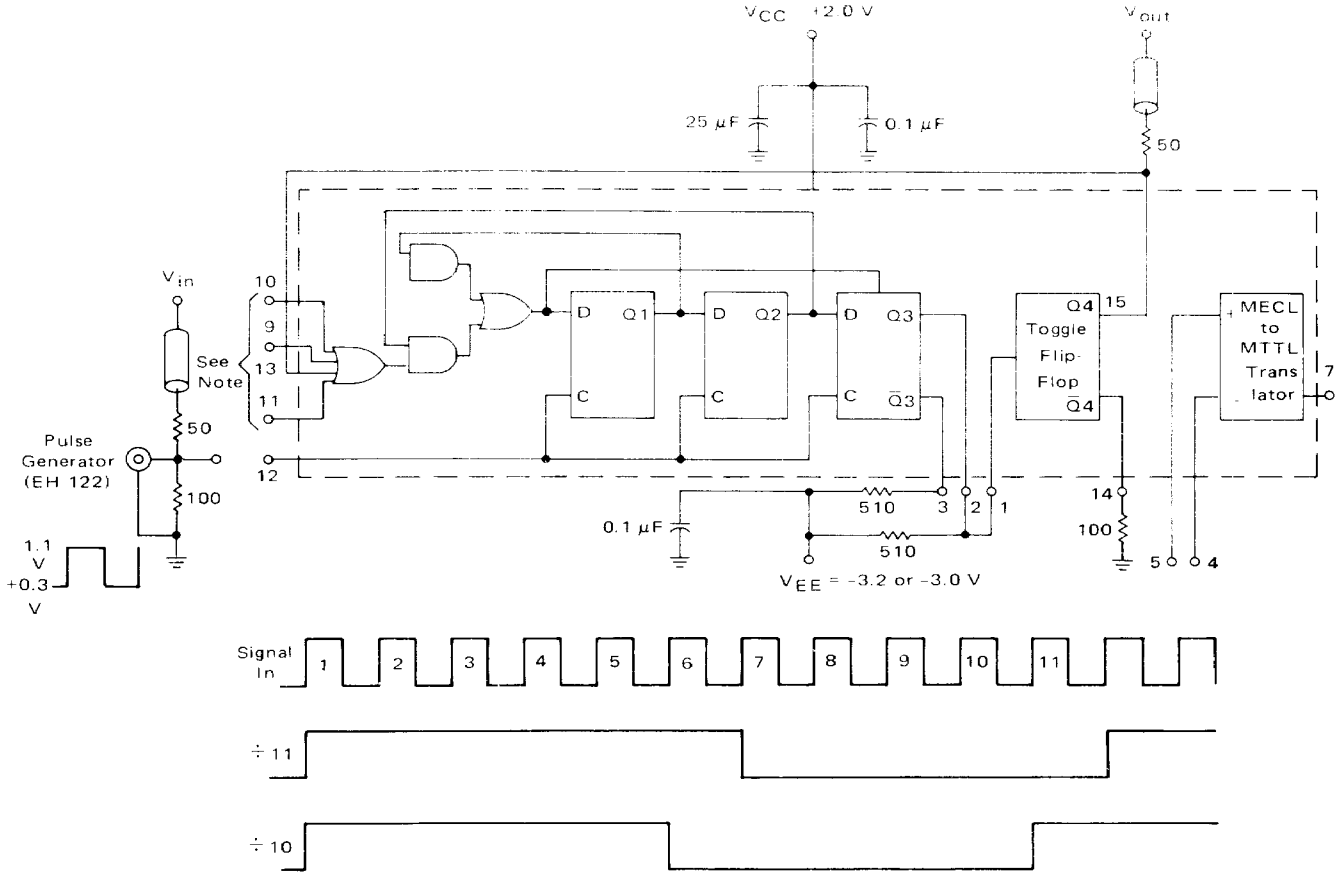


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT



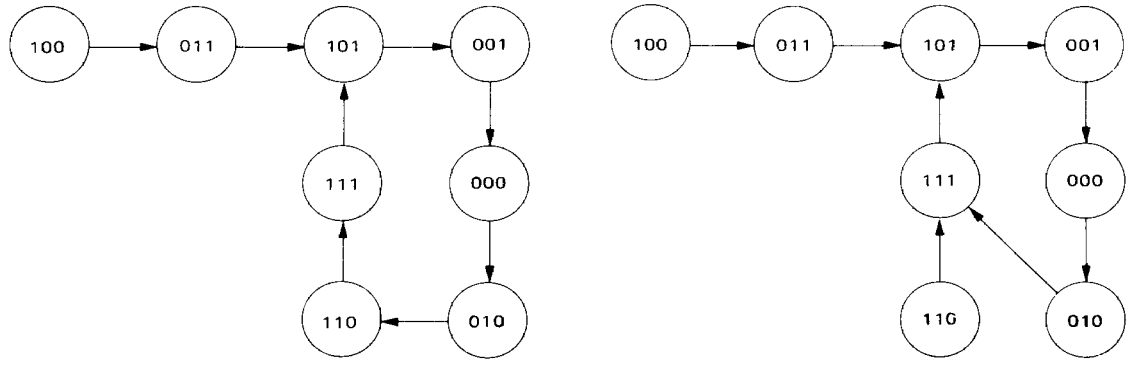
NOTE: Output Waveforms are same as shown in Figures 4 and 5.

FIGURE 7 – TOGGLE FREQUENCY TEST CIRCUIT



NOTE: For divide by 11 connect 11 to V_{IL} = +0.130 and 9 and 10 to V_F = -3.0 V
For divide by 10 connect 11 to V_{IH} = +1.160 or 9 or 10 to V_R = 0.0 V

FIGURE 8 – STATE DIAGRAMS



FUNCTION DESCRIPTION

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable ÷5/÷6 prescaler; 2) a ÷ 2 prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the ÷5 operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add t++ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The ÷ 5/÷ 6 prescaler may be connected externally to the ÷ 2 prescaler to form a ÷ 10/÷ 11 prescaler (Figure 10) or a ÷ 10/÷ 12 prescaler (Figure 11).

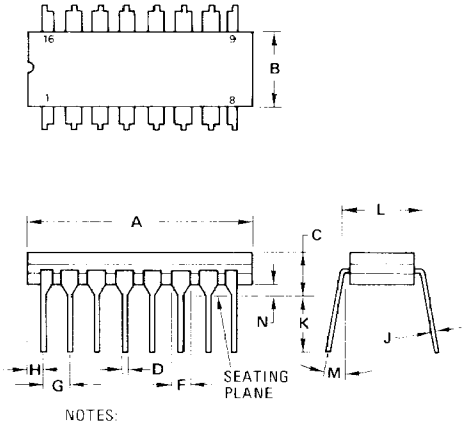
By way of an example showing how a ÷ 10/÷ 11 prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the ÷ 5/÷ 6 prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between ÷ 5 and ÷ 6 resulting in a ÷ 11 at Q4.

If any one or all of the E inputs are high (Figure 10), the 5/6 prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

OUTLINE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE
2. AT MAXIMUM MATERIAL CONDITION'
   PKG. INDEX: NOTCH IN LEAD
   NOTCH IN CERAMIC OR INK DOT'
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620

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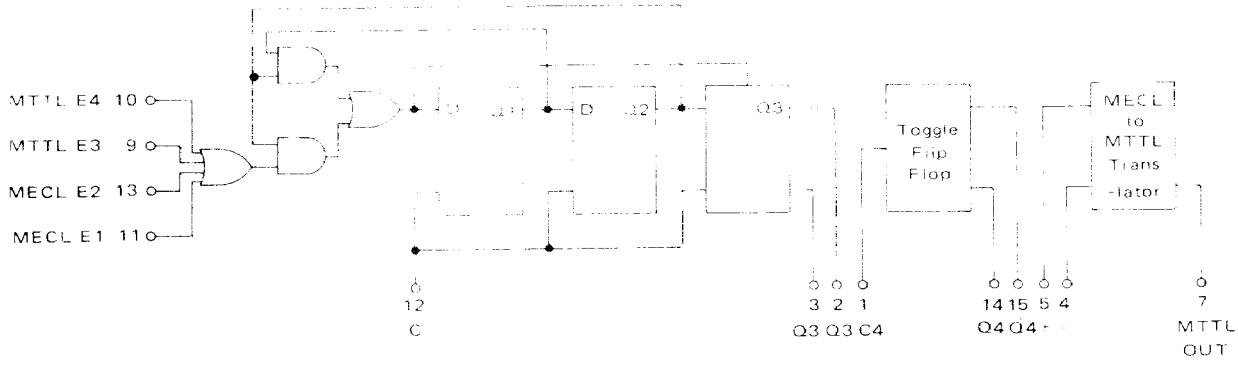
FIGURE 5 – ÷ 5/6



Divide by 2 use Toggle Flip Flop

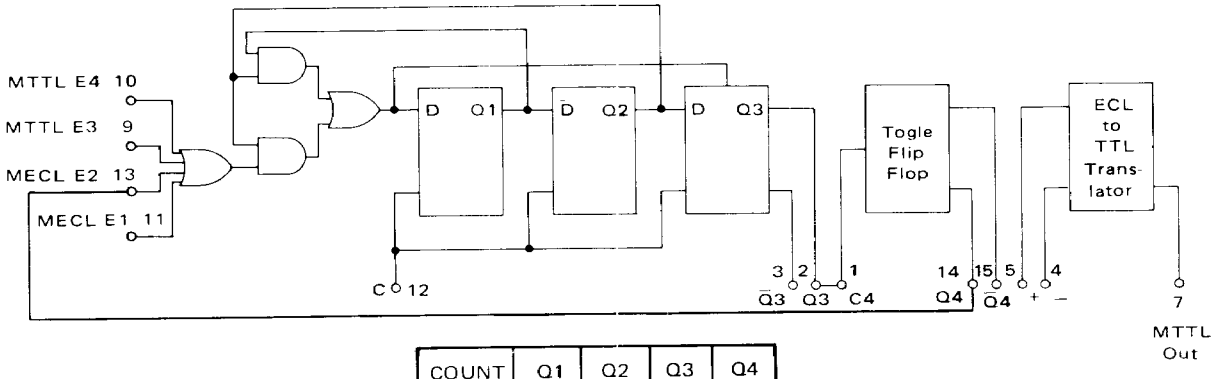
E1 + E2 + E3 + E4 = 1

E1 + E2 + E3 + E4 = 0

COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

To obtain an MTTL output connect 5 and 4 to 2 and 3 or 14 and 15, respectively.

FIGURE 10 – ÷ 10/11



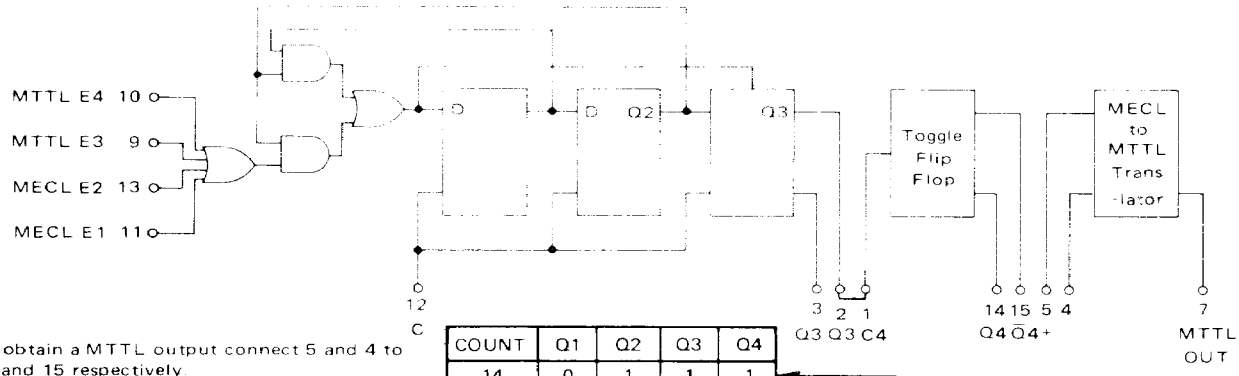
E1 + E3 + E4 = 1

E1 + E3 + E4 = 0

COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

To obtain an MTTL output connect 5 and 4 to 14 and 15, respectively.

FIGURE 11 – ÷10/12



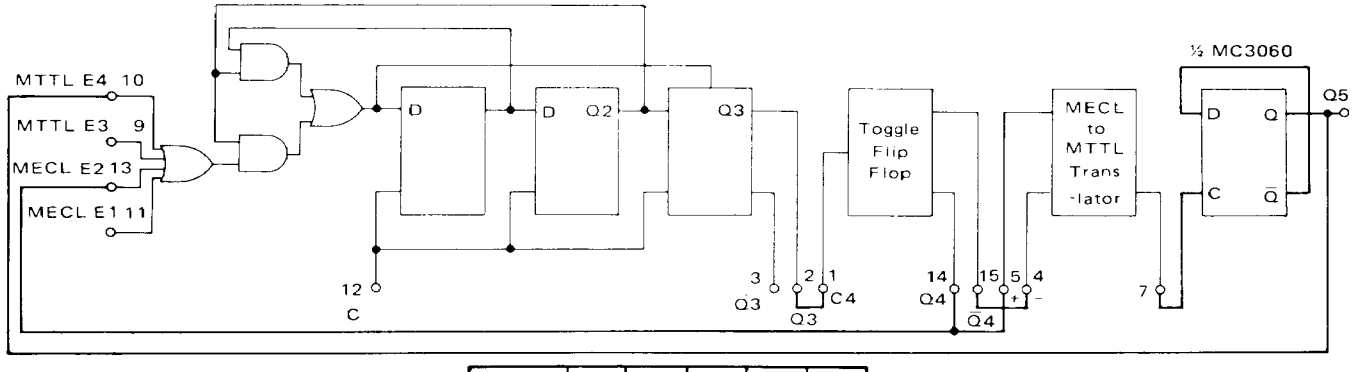
To obtain a MTTL output connect 5 and 4 to 14 and 15 respectively.

E1 + E2 + E3 + E4 = 1

E1 + E2 + E3 + E4 = 0

COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
6	0	1	1	0
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

FIGURE 12 – ÷20/21



To obtain a divide by 20/22 omit Q5 to 10.
To obtain a divide by 20/24 omit 14 to 13.

E1 + E3 = 1

E1 + E3 = 0

COUNT	Q1	Q2	Q3	Q4	Q5
31	0	1	1	1	1
30	1	1	1	1	1
29	1	0	1	1	1
25	1	0	0	1	1
24	0	0	0	1	1
26	0	1	0	1	1
23	1	1	1	0	1
21	1	0	1	0	1
17	1	0	0	0	1
16	0	0	0	0	1
18	0	1	0	0	1
15	1	1	1	1	0
13	1	0	1	1	0
9	1	0	0	1	0
8	0	0	0	1	0
10	0	1	0	1	0
7	1	1	1	0	0
5	1	0	1	0	0
1	1	0	0	0	0
0	0	0	0	0	0
2	0	1	0	0	0