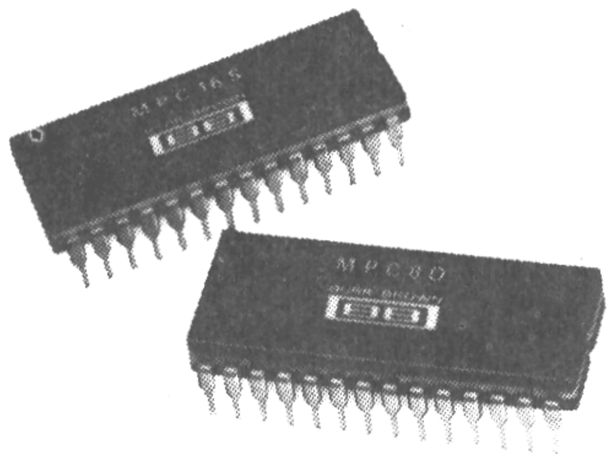
BURR-BROWN



# MPC8D
# MPC16S

## CMOS ANALOG MULTIPLEXERS

## FEATURES

- LOW POWER CONSUMPTION
  - CMOS analog switches
  - 15mW at 100kHz
  - 7.5mW standby power
- COMPACT DESIGN
  - Self-contained with internal channel address decoder
  - 8-channel dual (MPC8D) for differential inputs or
  - 16-channel (MPC16S) for single-ended inputs
  - 28-pin 0.600 inch-wide space-saving package
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- FAST SWITCHING SPEEDS PROVIDE HIGH THROUGHPUT RATES
  - 7µsec settling to 0.01%
  - 3µsec settling to 0.1%
- WIDE SUPPLY RANGE
  - ±7VDC to ±20VDC



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PDS-315

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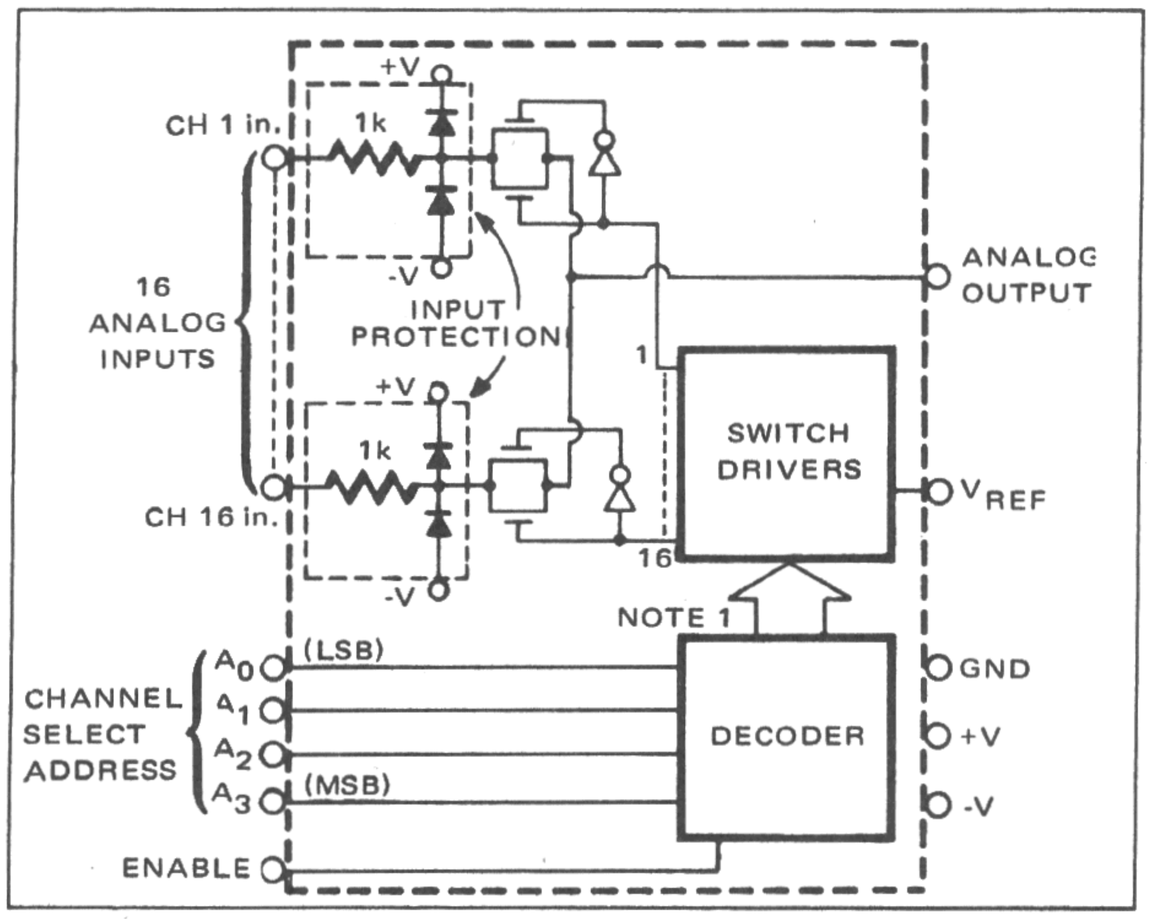
# DESCRIPTION

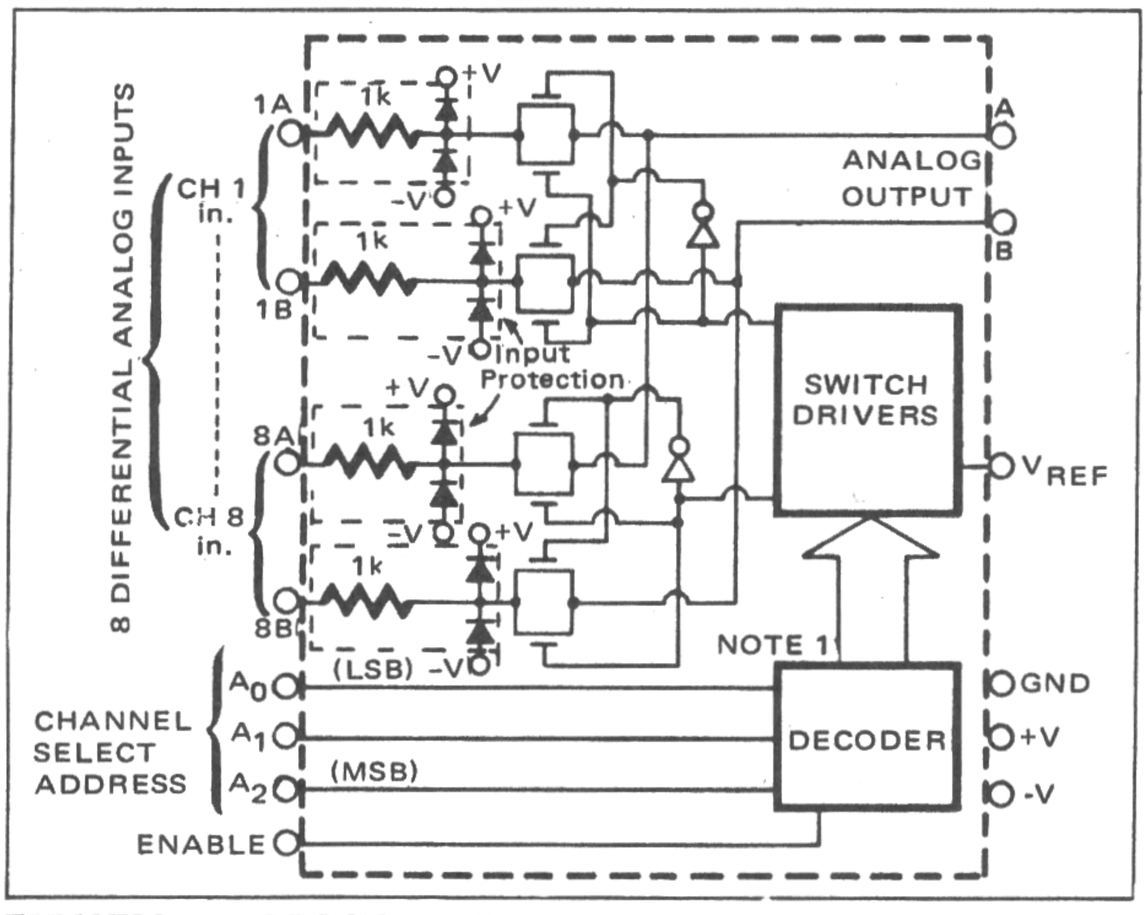
The MPC16S is single-ended monolithic 16 channel analog multiplexer and the MPC8D is a monolithic dual 8 channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ± 10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable a 16 channel group (MPC16S) or an 8 channel group (MPC8D) facilitating channel expansion in either single-node or multi-tiered matrix configurations.

Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.




FUNCTIONAL BLOCK DIAGRAM–MPC16S

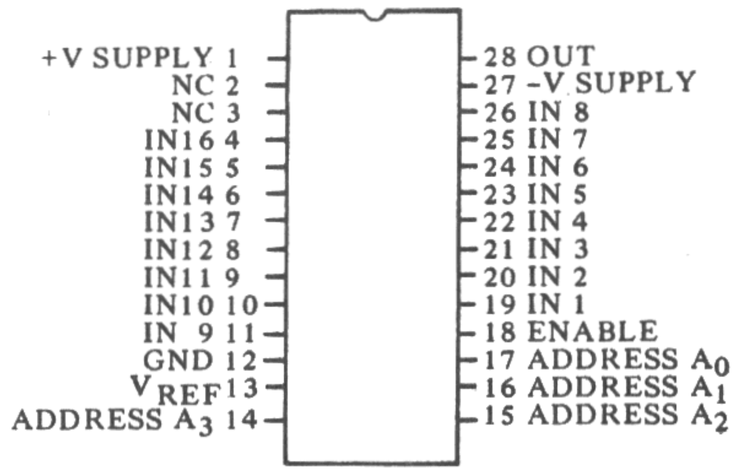



FUNCTIONAL BLOCK DIAGRAM–MPC8D

NOTE: 1 Inputs protected.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

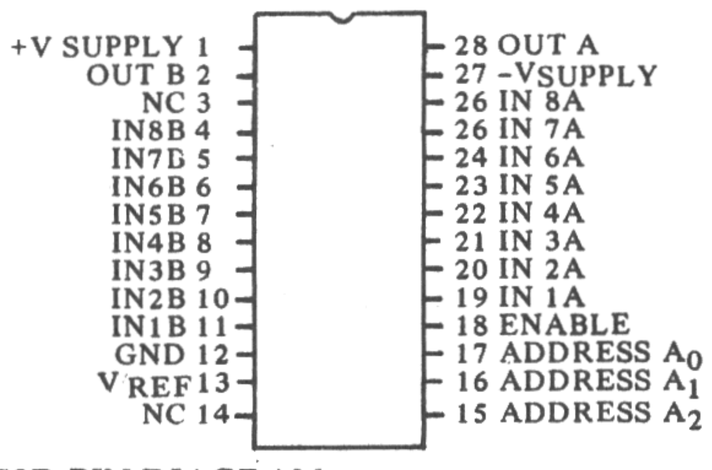
These devices are housed in compact 28 pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 506/507 series.




MPC16S PIN DIAGRAM

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | EN | "ON" CHANNEL |
|---|---|---|---|---|---|
| X | X | X | X | L | NONE |
| L | L | L | L | H | 1 |
| L | L | L | H | H | 2 |
| L | L | H | L | H | 3 |
| L | L | H | H | H | 4 |
| L | H | L | L | H | 5 |
| L | H | L | H | H | 6 |
| L | H | H | L | H | 7 |
| L | H | H | H | H | 8 |
| H | L | L | L | H | 9 |
| H | L | L | H | H | 10 |
| H | L | H | L | H | 11 |
| H | L | H | H | H | 12 |
| H | H | L | L | H | 13 |
| H | H | L | H | H | 14 |
| H | H | H | L | H | 15 |
| H | H | H | H | H | 16 |

TRUTH TABLE–MPC16S




MPC8D PIN DIAGRAM

| $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH PAIR |
|---|---|---|---|---|
| X | X | X | L | NONE |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

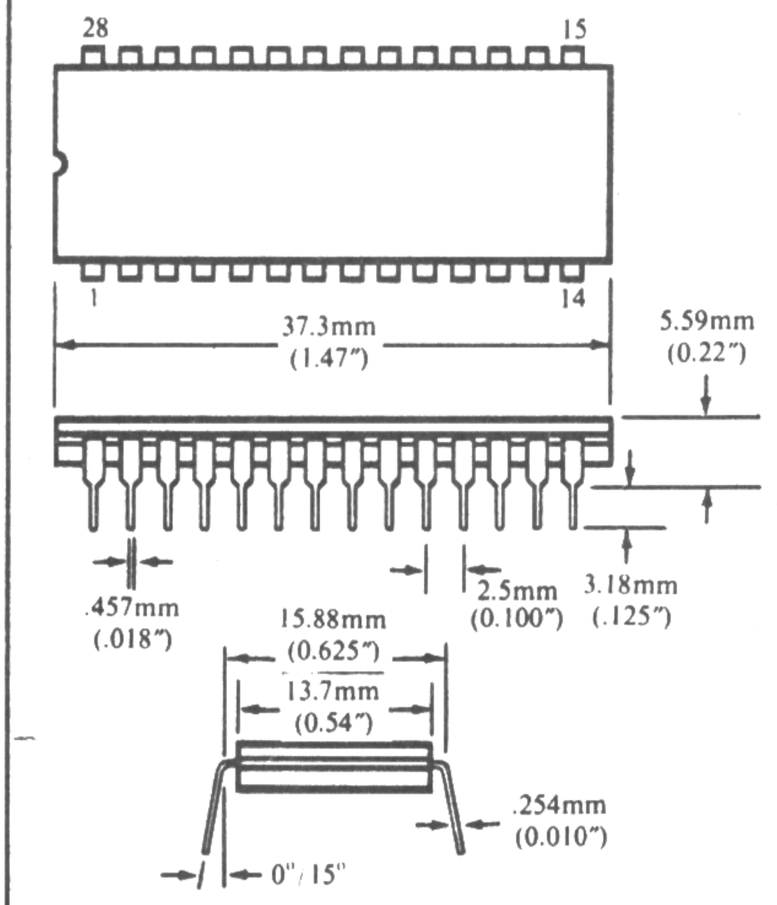
TRUTH TABLE–MPC8D

# ELECTRICAL SPECIFICATIONS

Typical for following conditions:
$V+ = +15$ V, $V- = -15$ V, $R_{source} \leq 1000\ \Omega$, $T_A = 25^oC$ unless otherwise noted.

| MODELS | MPC16S | MPC8D | Units |
|---|---|---|---|
| **INPUT** | | | |
| **ANALOG INPUT** | | | |
| Voltage Range | ±15 | | V |
| Maximum Overvoltage | +V supply +20 | | V |
| | -V supply -20 | | V |
| Current at Maximum Overvoltage per Channel (1) | ±18 | | mA |
| Number of Input Channels | | | |
| Single-Ended | 16 | | |
| Differential | | 8 | |
| Reference Voltage Range(2) | +6 to +10 | | V |
| ON Characteristics | | | |
| ON Resistance ($R_{ON}$) | | | |
| Typical | 1.3 | | kΩ |
| Maximum | 1.8 | | kΩ |
| $R_{ON}$ Drift vs. Temperature (0°C to +75°C) | 0.25 | | %/°C |
| $R_{ON}$ Mismatch | | | |
| Channel-to-channel | 50 | 50 | Ω |
| Differential | N/A | 50 | Ω |
| Input Leakage ($I_L$) | 1.0 | | nA |
| Input Leakage Drift | See Figure 9 | | |
| OFF Characteristics | | | |
| OFF Resistance | $10^{11}$ | | Ω |
| Output Leakage (all channels disabled) | 0.2 | | nA |
| Input Leakage (7) | 0.02 | | nA |
| Leakage Drift | See Figure 9 | | |
| Output Leakage with Input Overvoltage | | | |
| of +35 V | 1 | | nA |
| of -35 V | 1 | | μA |
| **DIGITAL INPUTS** | | | |
| Logic "0" ($V_L$)(1)(3) | -V supply ≤ $V_L$ < 0.8 @ 1 nA | | V |
| Logic "1" ($V_H$)(1)(3) | +4 ≤ $V_H$ ≤ +$V_{supply}$ @ 1 nA | | V |
| Channel Select | 4 bit binary code – one of sixteen | 3 bit binary code – one of eight | |
| Enable | Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel. | | |
| **POWER REQUIREMENTS** | | | |
| Rated Power Supply Voltages | ±15 | | V |
| Supply Range | | | |
| + Supply | +7 to +20 | | V |
| - Supply | -7 to -20 | | V |
| Supply Drain | | | |
| At 1 MHz Switching Speed | +4, -2 | | mA |
| At 100 kHz Switching Speed | ±0.5 | | mA |
| Typical Power Consumption | | | |
| DC to 10 kHz | 7.5 | | mW |
| **DYNAMIC CHARACTERISTICS** | | | |
| Gain Error (20 MΩ load) maximum | 0.01 | | % |
| Crosstalk (4) | 0.005 | | % of OFF channel signal |
| Settling Time(5) | | | |
| To 2 mV (0.01%) | 7 | | μs |
| To 20 mV (0.10%) | 3 | | μs |
| Common-Mode Rejection (minimum) | N/A | 120 | dB |
| Switching Time | | | |
| Turn ON | 0.5 | | μs |
| Turn OFF | 0.3 | | μs |
| Recovery Time from Input Overvoltage Pulse of 35 V for 100 μsec | | | |
| To 0.01% | 150 | | μs |
| To 0.10% | 15 | | μs |
| **OUTPUT** | | | |
| Voltage Range | ±15 | | V |
| Capacitance to Ground | 50 | 30(6) | pF |
| Capacitance Mismatch | N/A | ±10 | % |
| **TEMPERATURE** | | | |
| Specification | 0 to +75 | | °C |
| Storage | -65 to +150 | | °C |

# MECHANICAL SPECIFICATIONS




**NOTES:**

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to one watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Reference voltage controls noise immunity level. Normally not used (pin 13 left open).
3. Maximum overvoltage is ±$V_{supply}$ ±4 volts @ ±15 mA. Logic levels specified are for $V_{REF}$ (pin 13) open. For $V_{REF}$ = +10 V, $V_{H\ MIN}$ = +6 V.
4. 20 volt peak-peak 1000 Hz sinewave; $R_{source}$ = 1000 Ω, same signal on all unused channels.
5. For 20 volts between switched channels, $R_{source}$ = 1000 Ω. See Figure 5 for settling time vs. source impedance ($R_S$).
6. From each side of MPC8D to ground.
7. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

# DISCUSSION OF PEFORMANCE

## STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance ($R_{ON}$), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

### SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8$ ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A $10^6$ ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a $10^8$ ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where } \begin{array}{l} R_S = R_{source} \\ R_L = \text{load resistance} \\ R_{ON} = \text{multiplexer ON resistance.} \end{array}$$

### INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as a result of the $I_R$ drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20$\mu$Volts if a 1000 ohm source is used, and 200$\mu$Volts if a 10,000 ohm source is used. In general, for the MPC16S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_{SOURCE})$$

where $I_b$ = Bias current of device multiplexer is driving
$I_L$ = Multiplexer leakage current
$R_{ON}$ = Multiplexer ON resistance
$R_{SOURCE}$ = Source resistance

### DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

### LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50 mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50 mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}$ ohms or higher.

### SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC8D is used for multiplexing high-level signals of 1 volt to 10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

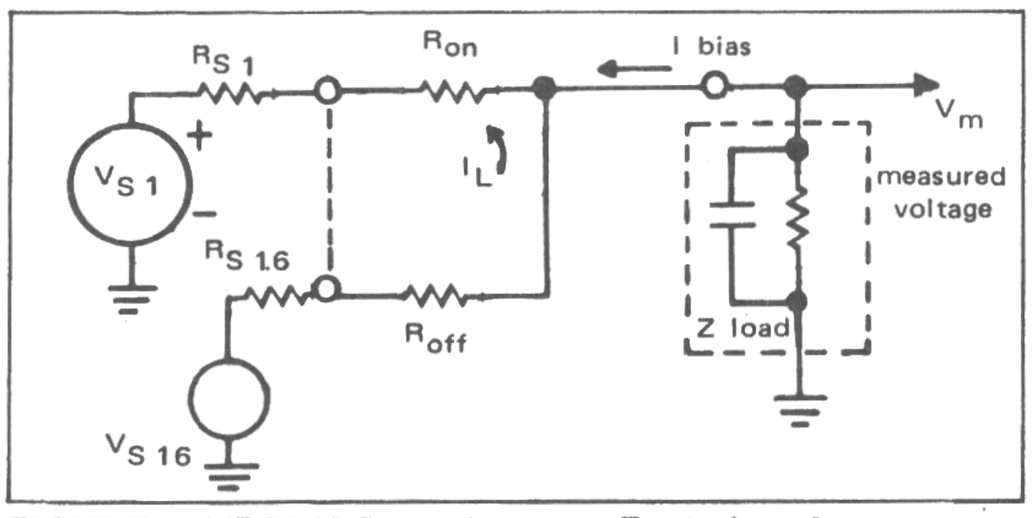



FIGURE 1: MPC16S Static Accuracy Equivalent Circuit.

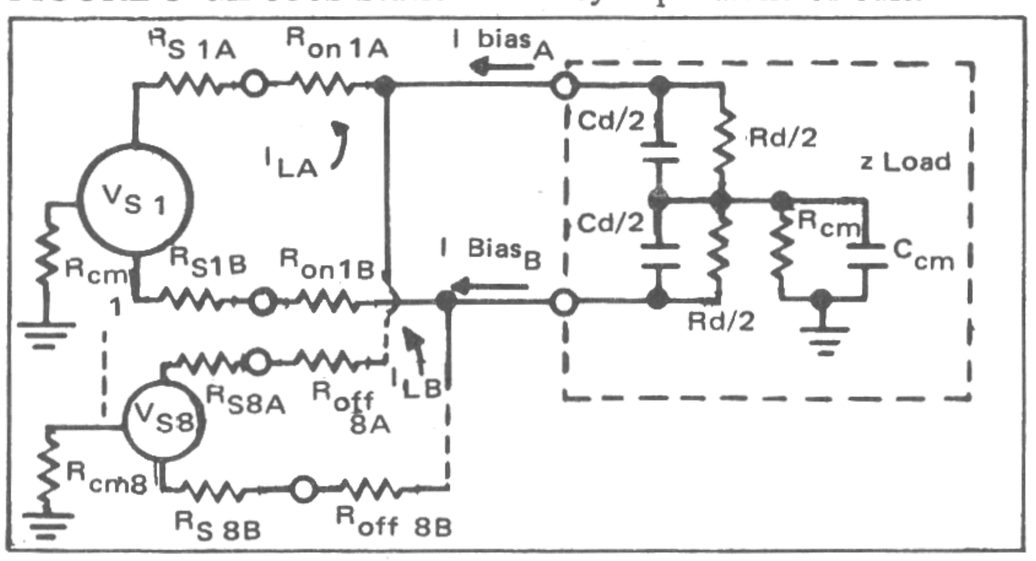



FIGURE 2: MPC-8D Static Accuracy Equivalent Circuit.

MUX MPC8D

# SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

## SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

## CROSSTALK

Crosstalk is the amount of signal feedthrough from the seven (MPC8D) or fifteen (MPC16S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the $R_{ON}$ and $R_{SOURCE}$ impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

## COMMON-MODE REJECTION (MPC8D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC8D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

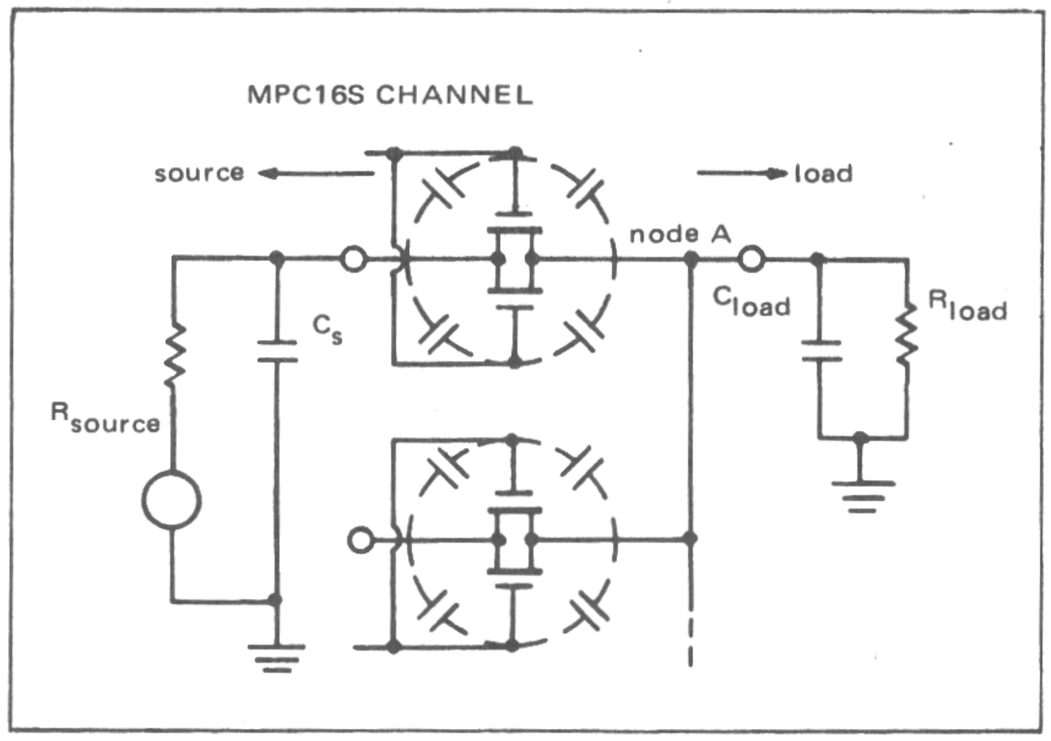



FIGURE 3: Settling Time Effects–MPC16S.

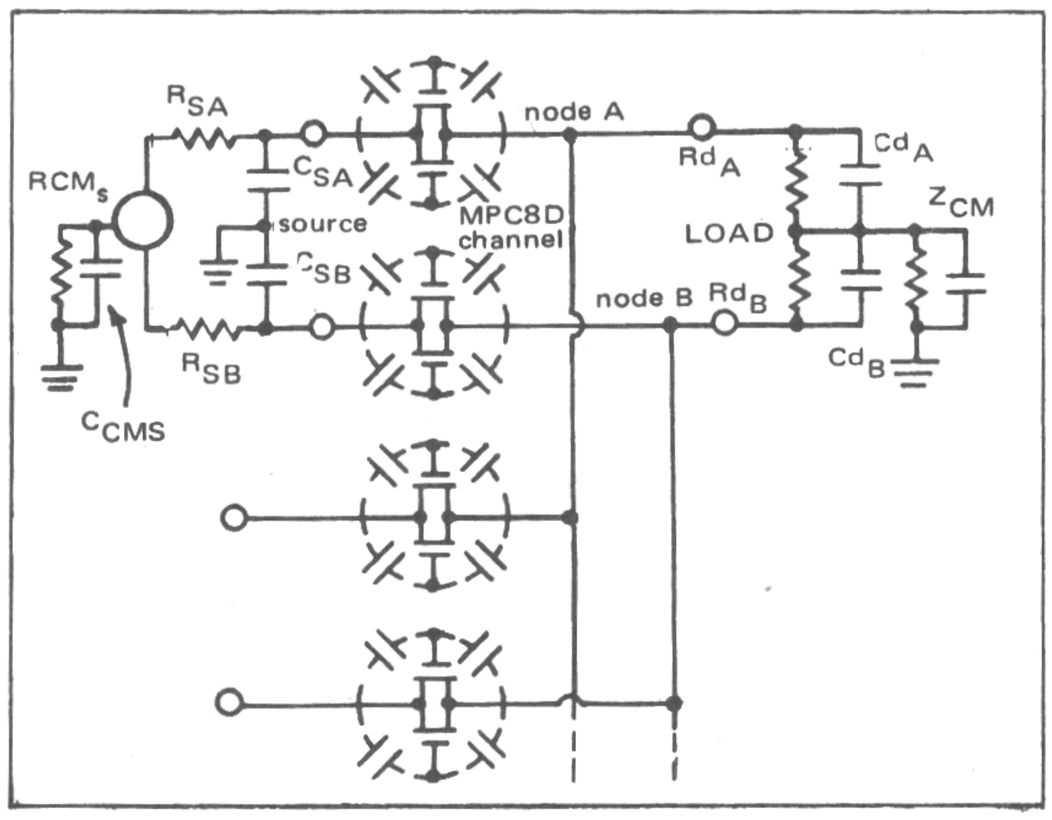



FIGURE 4: Settling & Common-Mode Effects–MPC-8D.

The CMR of the MPC8D and Burr-Brown's model 3660 Instrumentation Amplifier is 110 dB at DC to 1k Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 instrumentation amplifier connected for a gain of 1000 and with source unbalances of 10 k, 1 kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

# TYPICAL PERFORMANCE CURVES

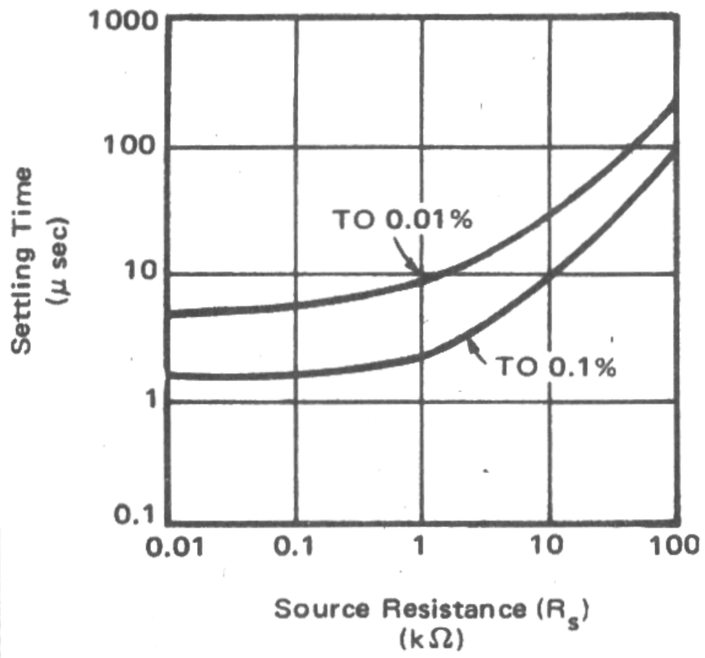



**FIGURE 5. Settling time vs source resistance for 20 volt step change.**

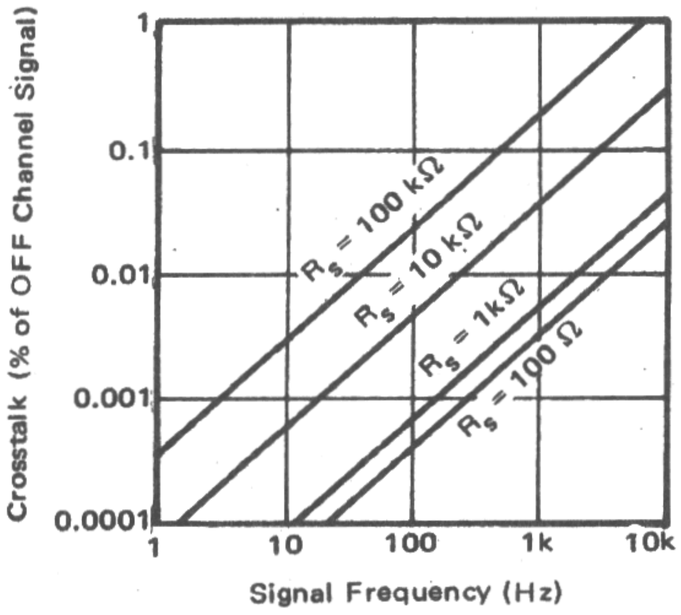



**FIGURE 6. Crosstalk vs signal frequency.**

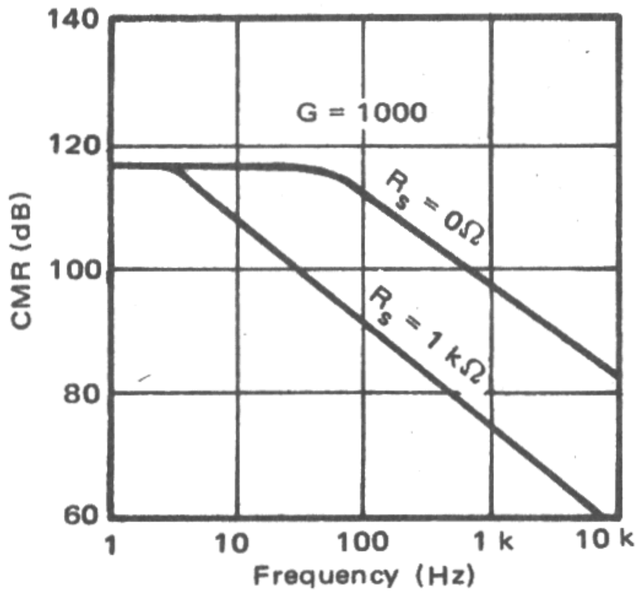



**FIGURE 8. Combined CMR vs. frequency for Model 3670 IA and MPC8D (G = 1000).**

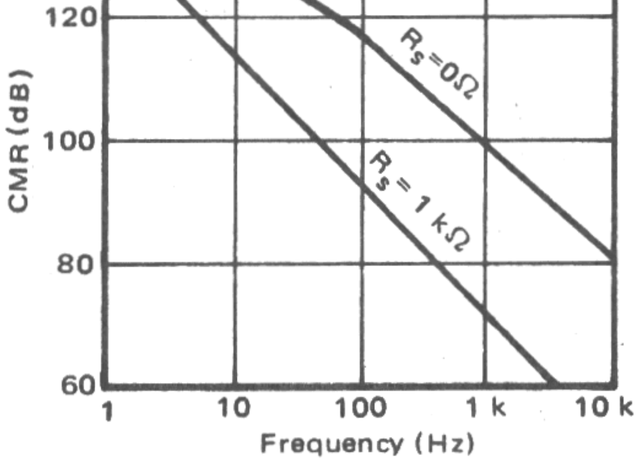



**FIGURE 7. CMR vs. frequency for Model 3660 IA and MPC8D (G = 1000).**

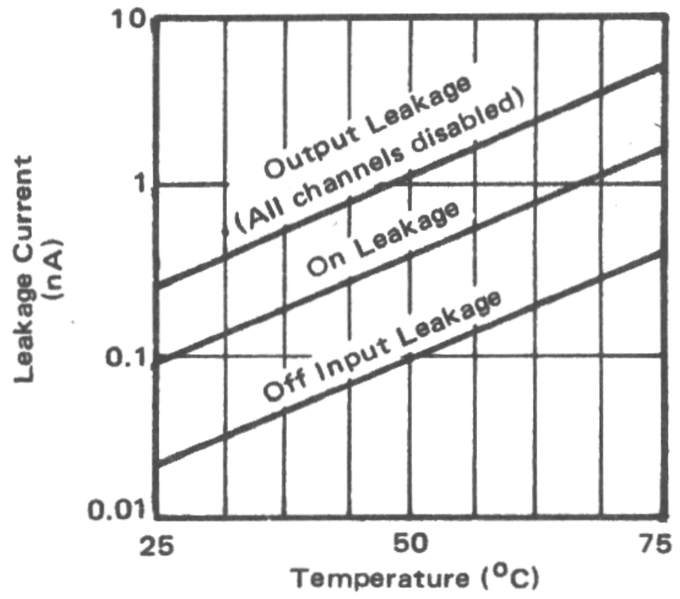



**FIGURE 9. Leakage current vs temperature.**

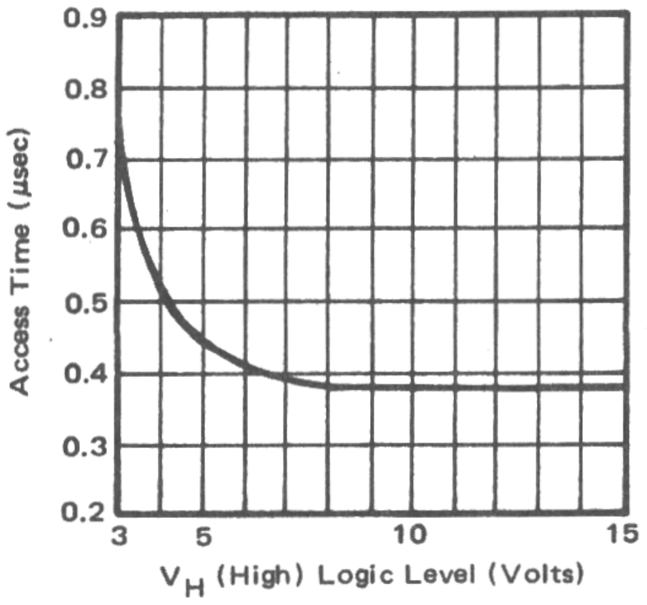



**FIGURE 10. Access time vs logic level (high).**

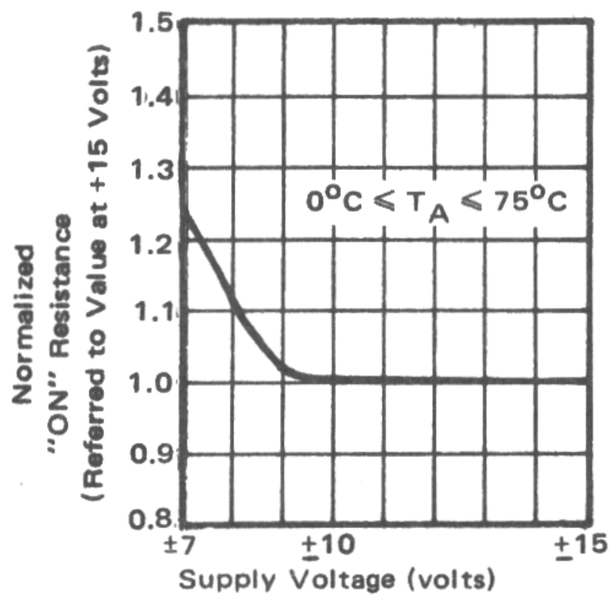



**FIGURE 11. Normalized "ON" resistance vs. supply voltage.**

# OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With the ENABLE line at a logic 1, the channel is selected by the 3 bit (MPC8D) or 4 bit (MPC16S) Channel Select Address (see the Truth Tables on page 5-143). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC8D and MPC16S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 5-144).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC8D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

# CHANNEL EXPANSION

## SINGLE ENDED MULTIPLEXER (MPC16S)

Up to 64 channels (4 multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC16S multiplexers on a two-tiered structure as shown in Figures 12 and 13.

## DIFFERENTIAL MULTIPLEXER (MPC8D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or 8 x 8 configuration.

## SINGLE NODE EXPANSION

The 64 x 1 configuration is simply eight MPC8D units tied to a single node. Programming is accomplished with a 6 bit counter, using the 3 LSB's of the counter to control Channel Address inputs $A_0$, $A_1$ and $A_2$ and the 3 MSB's of the counter to drive an 8 or 1 decoder. The 8 of 1 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC8D multiplexers.



## TWO TIER EXPANSION

Using an 8 x 8 2-tier structure for expansion to 64 channels, the programming is simplified. The 6 bit counter output does not require an 8 of 1 decoder. The 3 LSB's of the counter drive the $A_0$, $A_1$ and $A_2$ inputs of the eight first tier multiplexers and the 3 MSB's of the counter are applied to the $A_0$, $A_1$ and $A_2$ inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multi-tiered configuration.

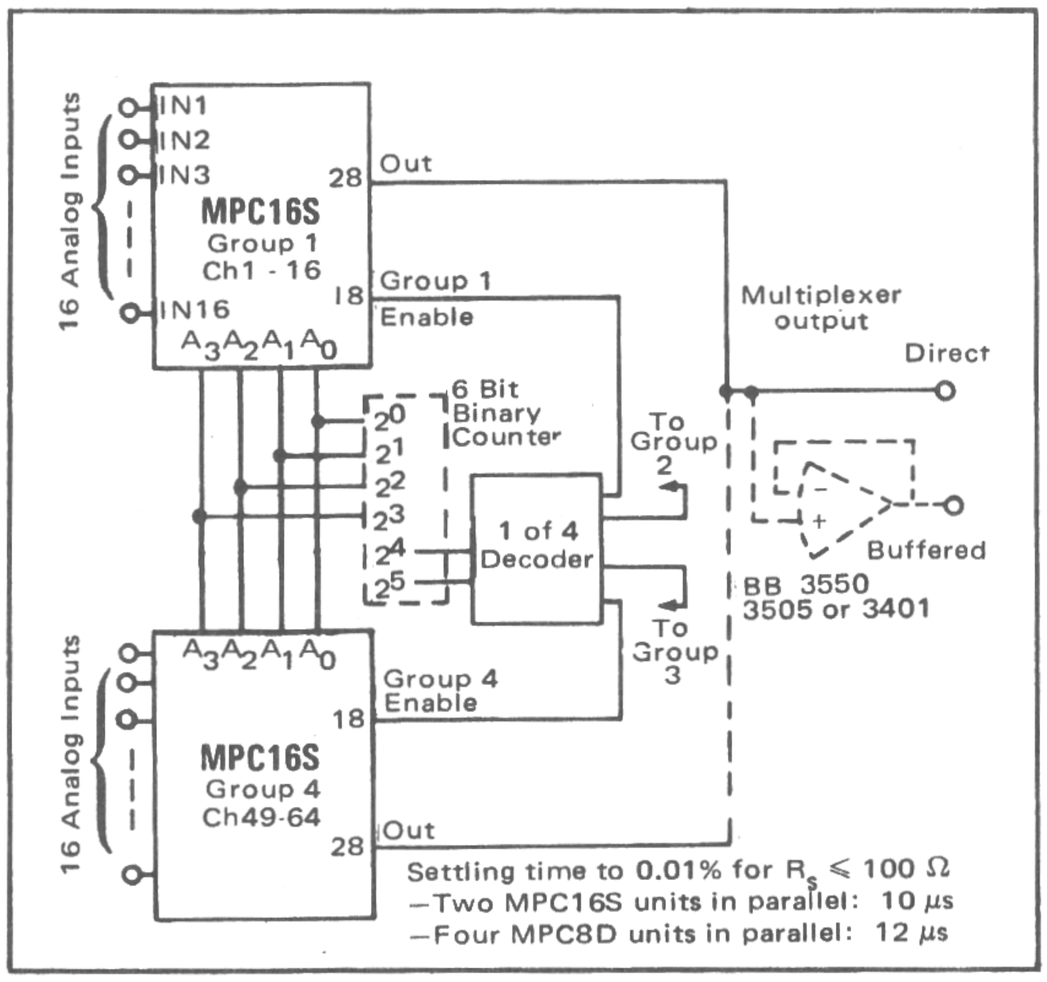



FIGURE 12. 32 To 64 Channel, Single-Tier Expansion.

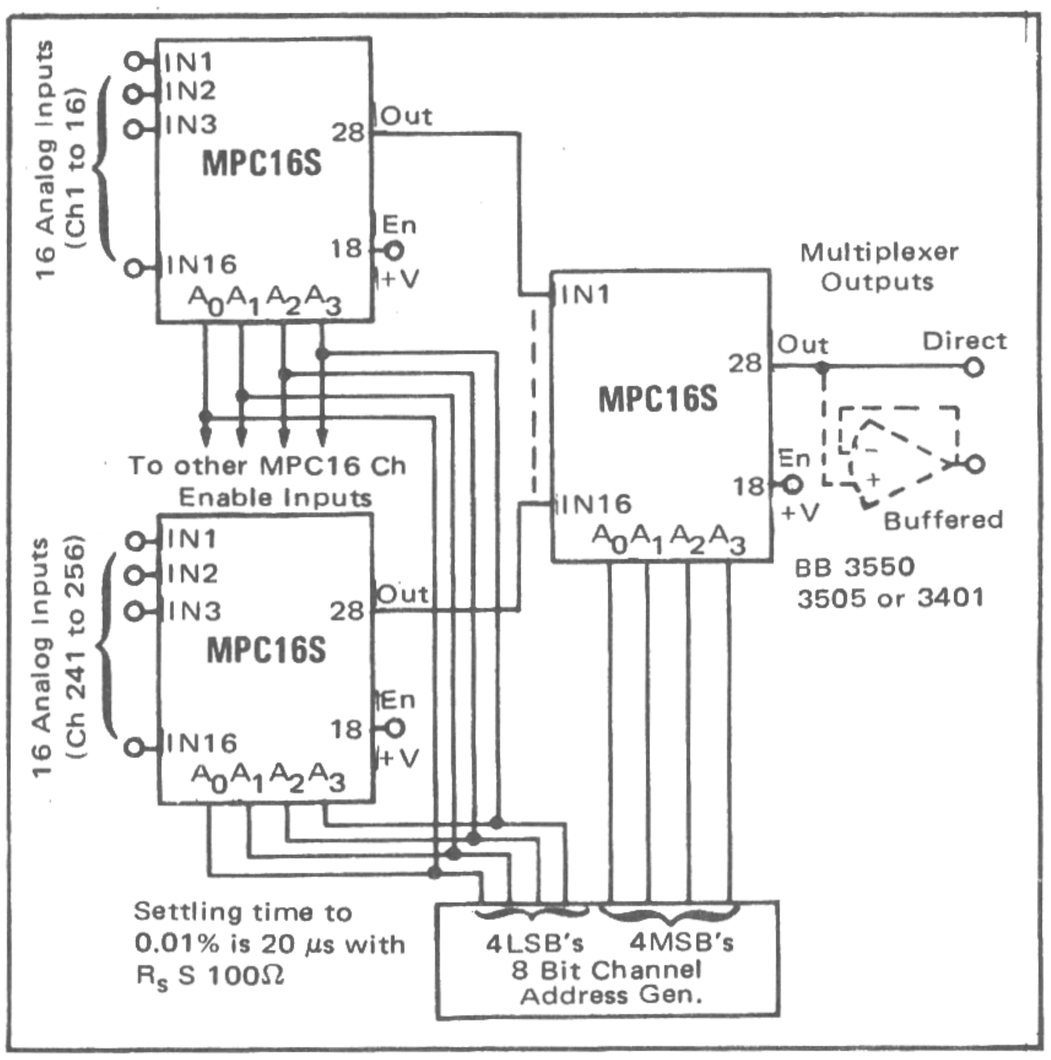



FIGURE 13. Channel Expansion Up To 256 Channels Using 16 x 16 Two Tiered Expansion.