- **Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages**

- **Dependable Texas Instruments Quality and Reliability**
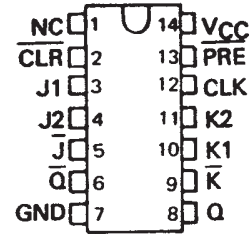
description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.
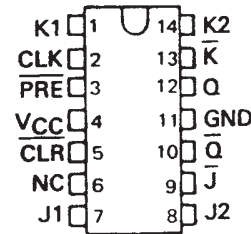
These flip-flops are ideally suited for medium-to-high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

The SN5470 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN7470 is characterized for operation from 0°C to 70°C.

SN5470 . . . J PACKAGE
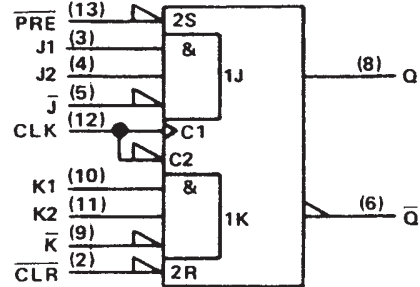**SN7470 . . . N PACKAGE**
(TOP VIEW)

```
        ____
NC   [1  U  14] VCC
CLR  [2     13] PRE
J1   [3     12] CLK
J2   [4     11] K2
J    [5     10] K1
Q    [6      9] K
GND  [7      8] Q
```

SN5470 . . . W PACKAGE
(TOP VIEW)

```
        ____
K1   [1  U  14] K2
CLK  [2     13] K
PRE  [3     12] Q
VCC  [4     11] GND
CLR  [5     10] Q
NC   [6      9] J
J1   [7      8] J2
```

NC – No internal connection

logic symbol[†]


```
PRE  (13)  →  2S
J1   (3)   →  &
J2   (4)   →       1J     (8)  Q
J    (5)   →
CLK  (12)  → ▷C1
              C2
K1   (10)  →  &
K2   (11)  →       1K     (6)  Q
K    (9)   →
CLR  (2)   →  2R
```

[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages only.

positive logic

$$J = J1 \cdot J2 \cdot \overline{J}$$
$$K = K1 \cdot K2 \cdot \overline{K}$$

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L[†]	L[†]
H	H	↑	L	L	Q_0	$\overline{Q_0}$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q_0	$\overline{Q_0}$

If inputs J and K are not used, they must be grounded. Preset or clear function can occur only when the clock input is low.
[†]This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.
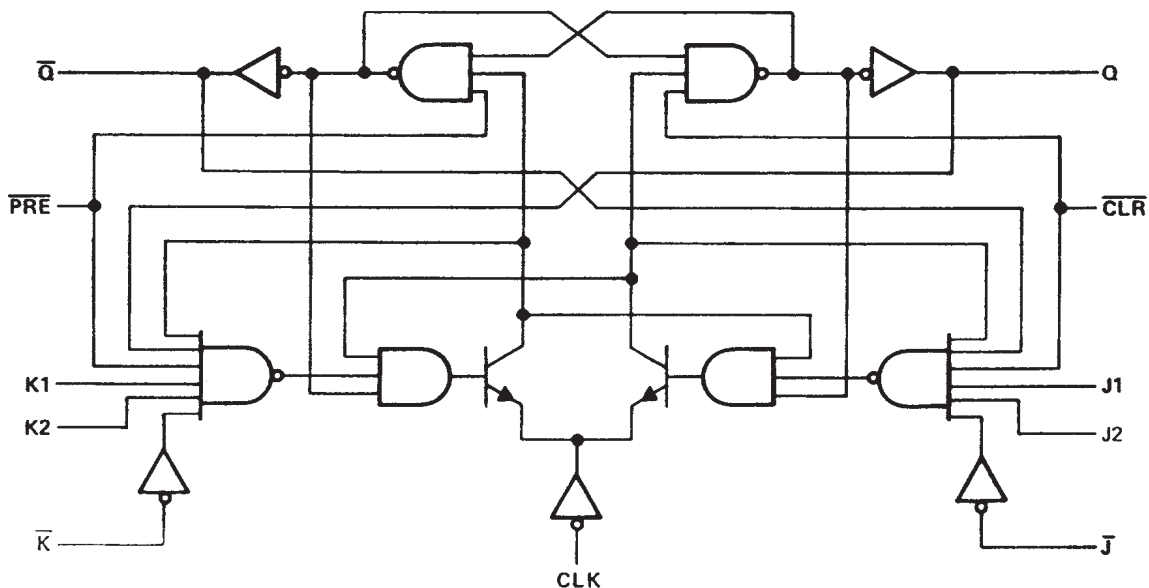
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logic diagram (positive logic)

'70-GATED J-K WITH CLEAR AND PRESET

schematics of input and outputs
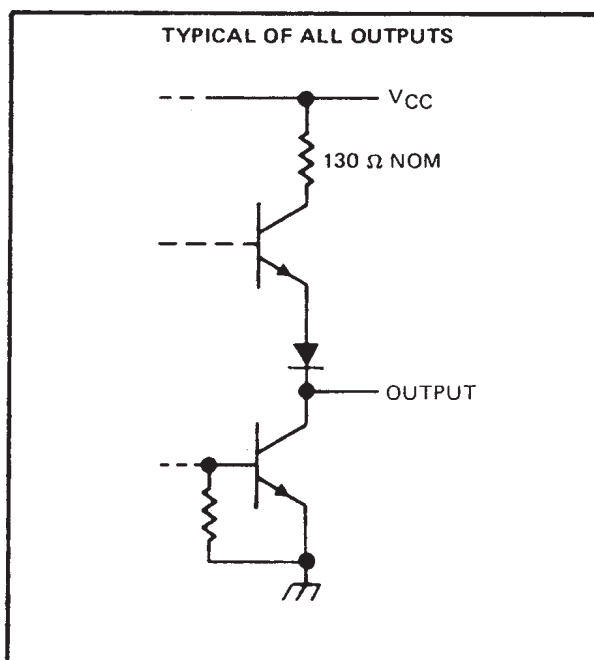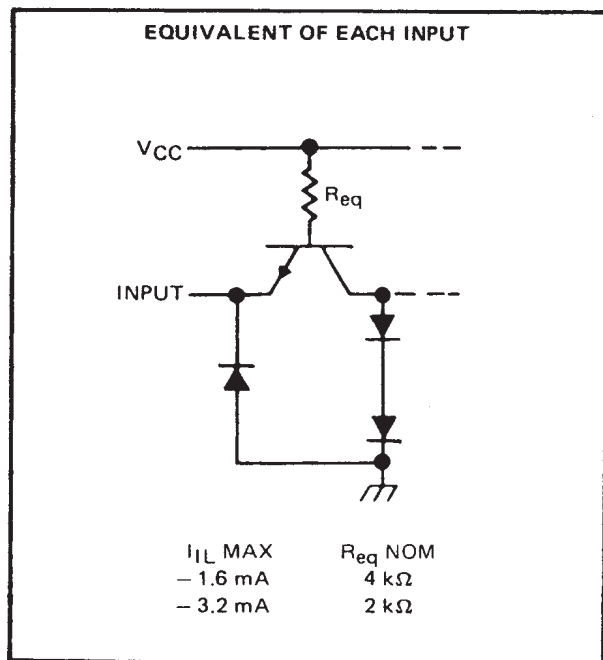
EQUIVALENT OF EACH INPUT

I_{IL} MAX	R_{eq} NOM
– 1.6 mA	4 kΩ
– 3.2 mA	2 kΩ

TYPICAL OF ALL OUTPUTS

130 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V

Input voltage .... 5.5 V

Operating free-air temperature: SN5470 .... $-55°C$ to $125°C$

SN7470 .... $0°C$ to $70°C$

Storage temperature range .... $-65°C$ to $150°C$

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5470			SN7470			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				-0.4			-0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	30			30			
		PRE or CLR low	25			25			
t_{su}	Setup time before CLK ↑		20			20			ns
t_h	Hold time-Data after CLK ↑		5			5			ns
T_A	Operating free-air temperature		-55		125	0		70	$°C$

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN5470			SN7470			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		$V_{CC} = $ MIN,	$I_I = -12$ mA			-1.5			-1.5	V
V_{OH}		$V_{CC} = $ MIN, $V_{IH} = 2$ V,	$V_{IL} = 0.8$ V, $I_{OH} = -0.4$ mA	2.4	3.4		2.4	3.4		V
V_{OL}		$V_{CC} = $ MIN, $V_{IH} = 2$ V,	$V_{IL} = 0.8$ V, $I_{OL} = 16$ mA		0.2	0.4		0.2	0.4	V
I_I		$V_{CC} = $ MAX,	$V_I = 5.5$ V			1			1	mA
I_{IH}	PRE or CLR	$V_{CC} = $ MAX,	$V_I = 2.4$ V			80			80	μA
	All other					40			40	
I_{IL}	PRE or CLR[¶]	$V_{CC} = $ MAX,	$V_I = 0.4$ V			-3.2			-3.2	mA
	All other					-1.6			-1.6	
I_{OS}[§]		$V_{CC} = $ MAX		-20		-57	-18		-57	mA
I_{CC}		$V_{CC} = $ MAX,	See Note 2		13	26		13	26	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

[§] Not more than one output should be shorted at a time.

[¶] Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER[†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}					20	35		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	R_L = 400 Ω,	C_L = 15 pF			50	ns
t_{PHL}							50	ns
t_{PLH}	CLK	Q or $\overline{Q}$				27	50	ns
t_{PHL}						18	50	ns

[†] f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output;
t_{PHL} = propagation delay time, high-to-low level output.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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