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DM74LS193 Synchronous 4-Bit Binary Counter with Dual Clock

General Description

The DM74LS193 circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (rippleclock) counters.

The outputs of the four master-slave flip-flops are triggered by a LOW-to-HIGH level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held HIGH.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is LOW. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent

of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

Ordering Code:

Order Number	Package Number	Package Description
DM74LS193M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
DM74LS193N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



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Absolute Maximum Ratings(Note 1)

Operating Free Air Temperature Range	
Supply Voltage	

Input Voltage

Storage Temperature Range

 Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be you operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

 7V
 The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
Vcc	Supply Voltage	4.75	5	5.25	V	
/н	HIGH Level Input Voltage	2			V	
/ _{IL}	LOW Level Input Voltage			0.8	V	
ОН	HIGH Level Output Current			-0.4	mA	
OL	LOW Level Output Current			8	mA	
f _{CLK}	Clock Frequency (Note 2)	0		25	MHz	
	Clock Frequency (Note 3)					
N	Pulse Width of any Input (Note 4)	20			ns	
SU	Data Setup Time (Note 4)	20			ns	
Н	Data Hold Time (Note 4)	0			ns	
EN	Enable Time to Clock (Note 4)	40			ns	
A	Free Air Operating Temperature	0		70	°C	

Note 2: C_L = 15 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 $k\Omega,~I_A$ = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
Symbol	Farameter	Conditions		(Note 5)		Units	
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 mA$			-1.5	V	
V _{OH}	HIGH Level Output	V _{CC} = Min, I _{OH} = Max	2.5	3.4		v	
	Voltage	V _{IL} = Max, V _{IH} = Min	2.7	3.4			
V _{OL}	LOW Level Output	V _{CC} = Min, I _{OL} = Max		0.25	0.4		
	Voltage	V _{IL} = Max, V _{IH} = Min		0.35	0.5	V	
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$		0.25	0.4		
I _I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			0.1	mA	
I _{IH}	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ	
IIL	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA	
I _{OS}	Short Circuit	V _{CC} = Max	-20		-100	mA	
	Output Current	(Note 6)	-20		-100		
I _{CC}	Supply Current	V _{CC} = Max (Note 7)		19	34	mA	

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second. Note 7: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Symbol	Parameter	From (Input)	$R_L = 2 k\Omega$						
		To (Output)	C _L = 15 pF		C _L = 50 pF		Units		
			Min	Max	Min	Max	1		
f _{MAX}	Maximum Clock Frequency		25		20		MHz		
t _{PLH}	Propagation Delay Time	Count Up		26		30			
	LOW-to-HIGH Level Output	to Carry				30	ns		
t _{PHL}	Propagation Delay Time	Count Up		24	24		36		
	HIGH-to-LOW Level Output	to Carry				24		36	ns
t _{PLH}	Propagation Delay Time	Count Down		24		29			
	LOW-to-HIGH Level Output		24		29	ns			
t _{PHL}	Propagation Delay Time	Count Down		24		32	ns		
	HIGH-to-LOW Level Output	to Borrow							
t _{PLH}	Propagation Delay Time	Either Count		20	38		45		
	LOW-to-HIGH Level Output	to Any Q		30		45	ns		
t _{PHL}	Propagation Delay Time	Either Count		47		54			
	HIGH-to-LOW Level Output	to Any Q		47	47		34	ns	
t _{PLH}	Propagation Delay Time	Load to		40		41			
	LOW-to-HIGH Level Output	Any Q			40	40		41	ns
t _{PHL}	Propagation Delay Time	Load to		40	40	1	47		
	HIGH-to-LOW Level Output	Any Q		40		47	ns		
t _{PHL}	Propagation Delay Time	Clear to		35	25	25	44	44	
	HIGH-to-LOW Level Output	Any Q				44	ns		

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