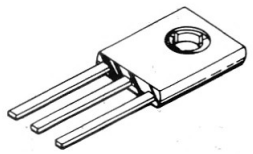
MOTOROLA

2N5193 (SILICON) thru 2N5195

Silicon PNP power transistors for use in power amplifier and switching circuits, – excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192.



CASE 77(1)

MAXIMUM RATINGS

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current	I_C	4.0			Adc
Base Current	I_B	1.0			Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	40 320			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	2N5193	$BV_{CEO(sus)}$*	40	-	Vdc
	2N5194		60	-	
	2N5195		80	-	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5193		-	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5194		-	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5195		-	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5193		-	0.1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5194		-	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5195		-	0.1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5193		-	2.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5194		-	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5195		-	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5193		-	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N5194		-	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5195		-	0.1	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	1.0	mAdc

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain*		h_{FE}*			-
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5193, 2N5194, 2N5195		25 20	100 80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5193, 2N5194, 2N5195		10 7.0	- -	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			-	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			-	1.4	
Base-Emitter On Voltage*		$V_{BE(on)}$*			Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			-	1.2	
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product		f_T			MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			2.0	-	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – NORMALIZED DC CURRENT GAIN

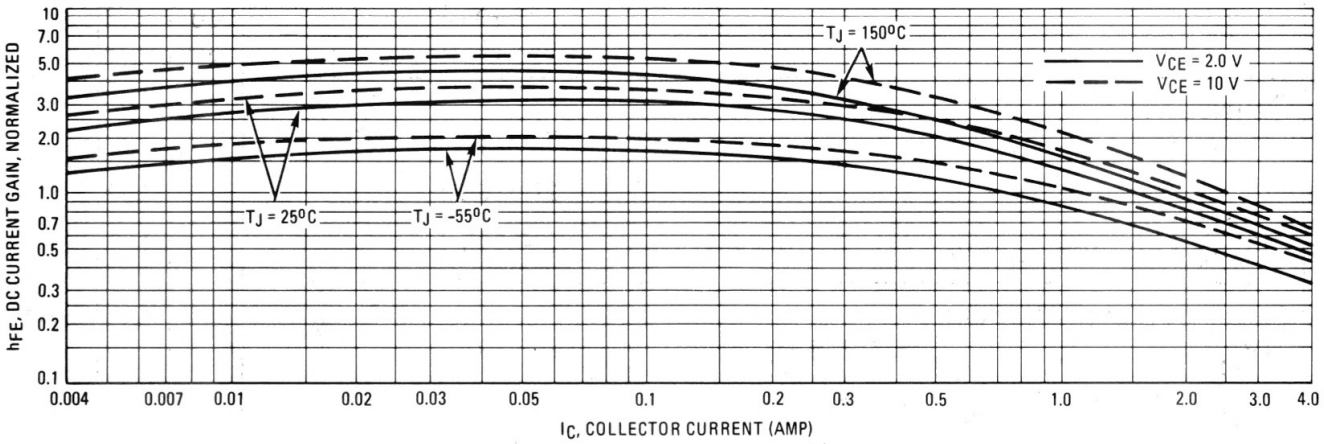
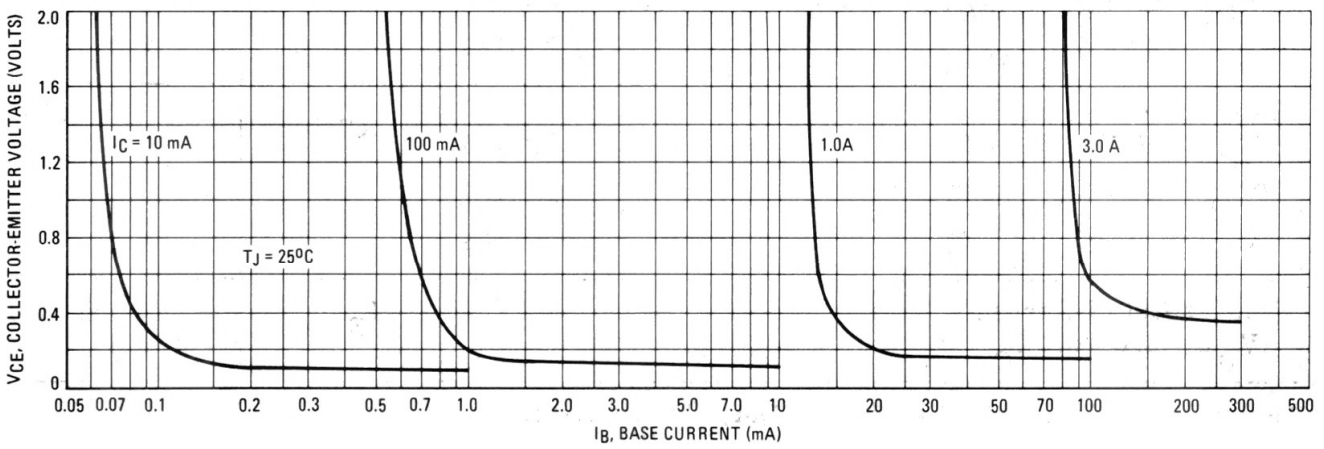


FIGURE 2 – COLLECTOR SATURATION REGION



2N5193 thru 2N5195 (continued)

FIGURE 3 – "ON" VOLTAGE

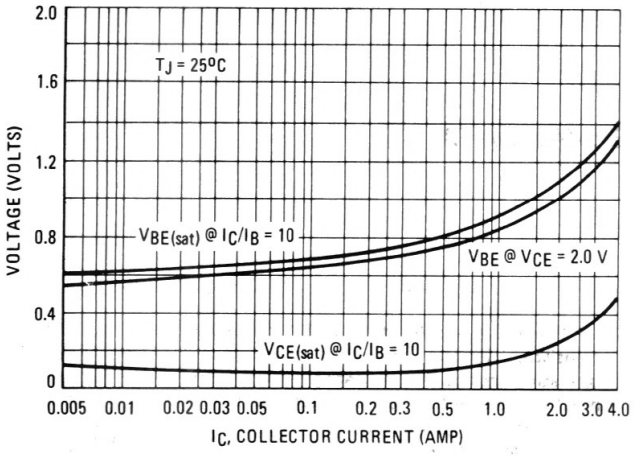
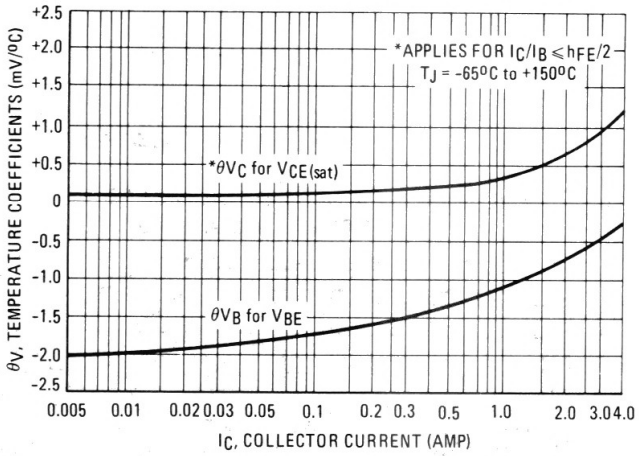


FIGURE 4 – TEMPERATURE COEFFICIENTS



TYPICAL "OFF" REGION CHARACTERISTICS

FIGURE 5 – COLLECTOR CUT-OFF REGION

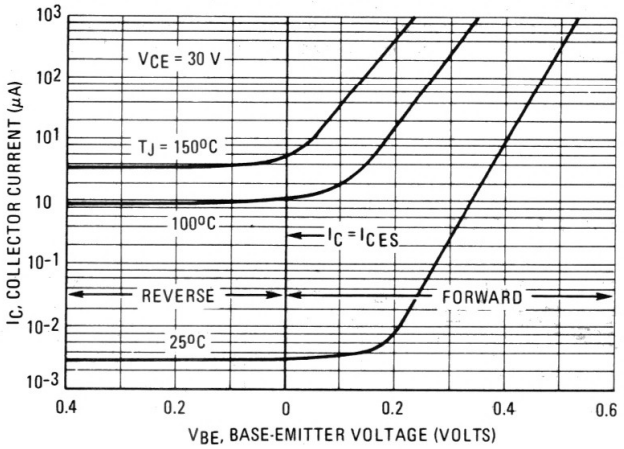


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

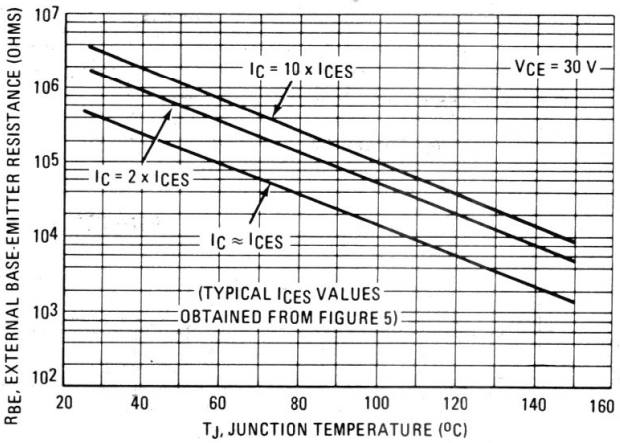


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

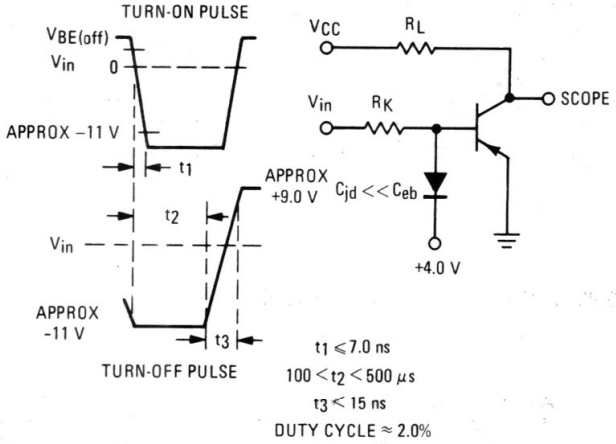


FIGURE 8 – CAPACITANCE

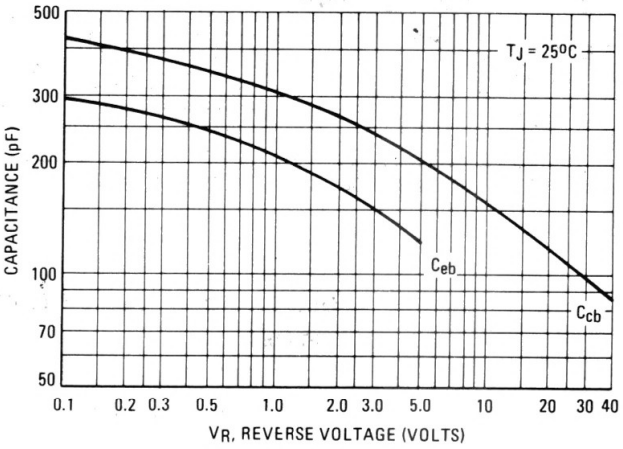


FIGURE 9 – TURN-ON TIME

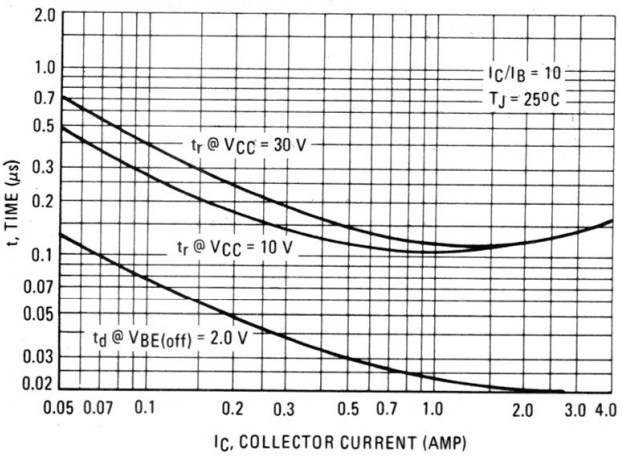
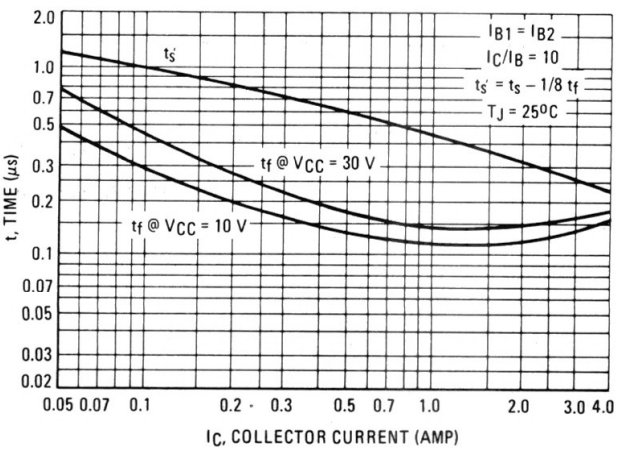
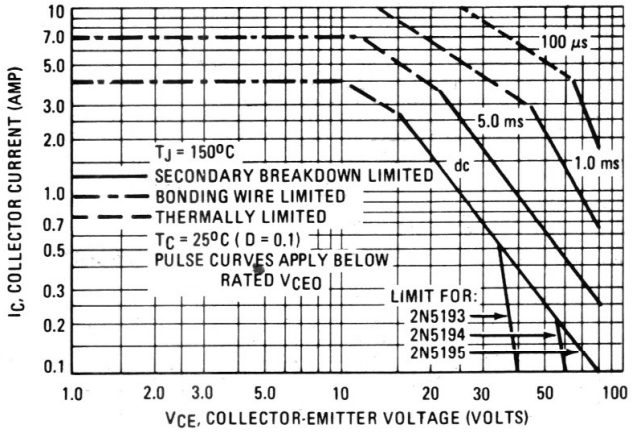


FIGURE 10 – TURN-OFF TIME



RATING AND THERMAL DATA

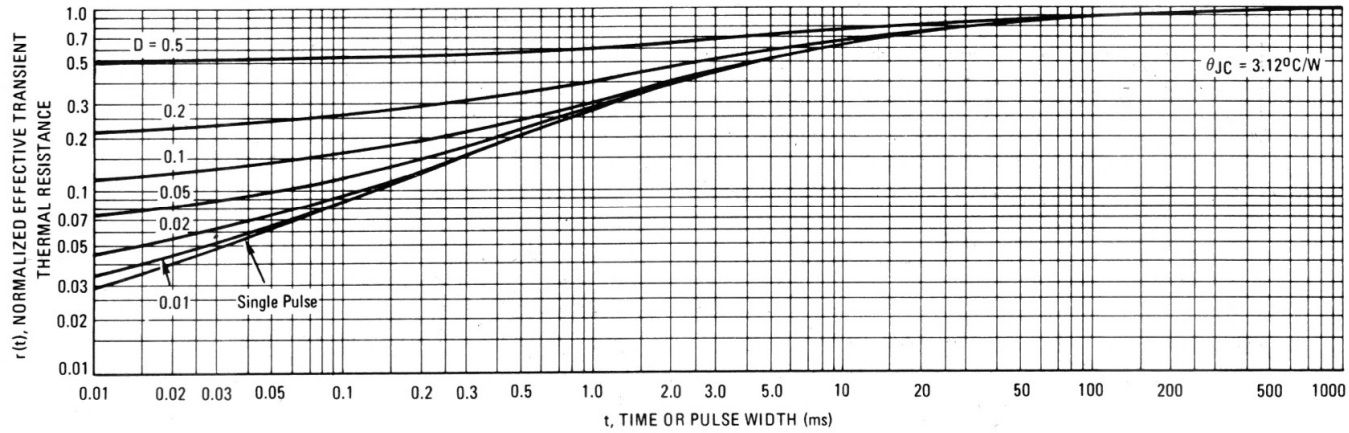
FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREAS



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

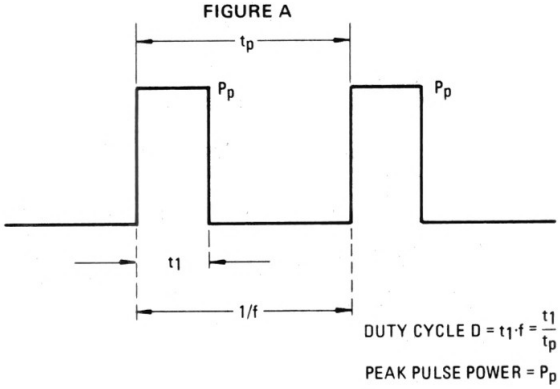
The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$