# **Bi-Directional Triode Thyristor**

# **Power Pac™ Triacs**

6A to 15A RMS Up to 600 Volts

Isolated and Non-Isolated Tab

A triac is a solid state silicon AC switch which may be gate triggered from an OFF-State to an ON-State for either polarity of applied voltage.

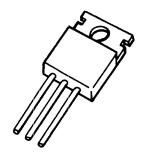
POWER PACTM triacs are molded silicone encapsulated devices which incorporate General Electric's patented POWER GLASTM glassivation process. This process provides an intimate bond between the silicon chip and the glass coating, significantly improving device performance and reliability. The copper mounting surface on the isolated tab types is electrically insulated from the silicon chip and the three electrical terminal leads.

#### **FEATURES:**

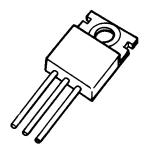
- POWER-GLASTM passivated silicon chip for maximum reliability.
- Very low off-state (leakage) current at room and elevated temperatures.
- Inherent immunity from non-repetitive transient voltage damage (max. critical rate-of-rise of on-state current subsequent to voltage breakover triggering, di/dt =  $10 \text{ A/}\mu\text{sec.}$ ).
- Low on-state voltage at high current levels.
- Excellent surge current capability.
- 1600 volts RMS Surge Isolation Voltage on Isolated Triacs.
- Selected types available from factory for use where circuit requires
  - with popular zero voltage triggering IC's
  - at 400 Hz
  - with low gate trigger current
  - at higher voltage levels
  - at higher commutating dv/dt levels

#### POWER PAC PACKAGE

- Meets JEDEC TO-220AB specifications.
- Round leads greatly simplifies assembly.
- Six standard lead forming configurations available from factory (including TO-66 compatibility.)

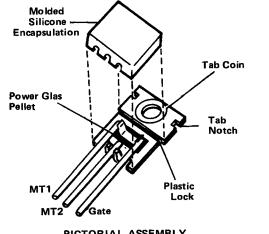


ISOLATED (RED)

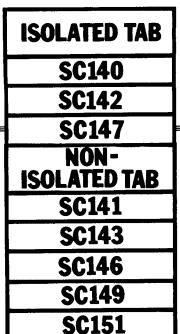


NON-ISOLATED (BLUE)

Rugged, industry-proven packaging.



PICTORIAL ASSEMBLY

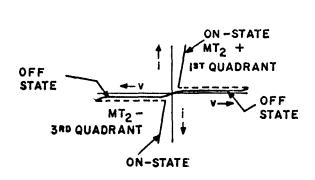


ISOLATED TAB	NON-ISOLATED TAB
SC140, 2, 7	SC141, 3, 6, 9, SC151

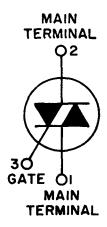
#### MAXIMUM ALLOWABLE RATINGS

	RMS ON-STATE CURRENT,	l .	REPETIT FF-STATE	VOLTA		SURGE (NON-I	FULL CYCLE REP) ON-STATE	I <sup>2</sup> t FOR FUSING FOR TIMES AT(3)		
TYPE	T(RMS) (1)		V <sub>DR</sub>	M <sup>(2)</sup>		CURRENT, IT	SM AMPERES	(RMS AMPERE)2	(RMS AMPERE)2	
	AMPERES	В	D	E	M	50 Hz	60 Hz	SECONDS 1.0	SECONDS, 8.3	
	AWIFERES	VOLTS	VOLTS	VOLTS	VOLTS	AMPERES	AMPERES	MILLISECOND	MILLISECONDS	
ISOLATED TAB										
SC140	6.5	200	400	500	600	74	80	18	26.5	
SC142	8	200	400	500	600	104	110	20	50	
SC147	10	200	400	500	600	104	110	20	50	
NON-ISO	NON-ISOLATED TAB									
SC141	6	200	400	500	600	74	80	18	26.5	
SC143	8	200	400	500	600	110	120	20	60	
SC146	10	200	400	500	600	110	120	20	60	
SC149	12	200	400	500	600	110	120	20	60	
SC151	15	200	400	500	600	110	120	20	60	

Peak Gate Power Dissipation, P <sub>GM</sub> (4)	10 Watts for 10 Microseconds (See Chart 4)
Average Gate Power Dissipation, P <sub>G(AV)</sub>	0.5 Watts
Peak Gate Current, I <sub>GM</sub> (4)	See Chart 4
Peak Gate Voltage, V <sub>GM</sub> (4)	See Chart 4
Storage Temperature, T <sub>stg</sub>	40°C to +125°C
Operating Temperature, T <sub>1</sub>	40 °C to +100 °C
Surge Isolation Voltage (5)	



TYPICAL CHARACTERISTICS VOLT-AMPERES



TERMINAL ARRANGEMENT

#### NOTES:

- At the case reference point (see outline drawing) temperature of 80°C maximum (except 75°C maximum for SC142 and SC149) and 360° conduction.
- 2. Ratings apply for zero gate voltage only. Ratings apply for either polarity of main terminal 2 voltage referenced to main terminal 1.
- 3. Ratings apply for either polarity of main terminal 2 referenced to main terminal 1.
- 4. Ratings apply for either polarity of gate terminal referenced to main terminal 1.
- 5. Isolated tab triacs only. Rating applies from main terminals 1 and 2 and gate terminal to device mounting surface. Test voltage is 50 or 60 Hz sinusoidal wave form applied for one minute. Rating applies over the entire device operating temperature range.

ISOLATED TAB	NON-ISOLATED TAE		
SC140, 2, 7	SC141, 3, 6, 9, SC151		

# **CHARACTERISTICS**

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	REF. NOTE
Repetitive Peak Off- State Current	I <sub>DRM</sub>				mA	V <sub>DRM</sub> = Maximum Allowable Repeti tive Off-State Voltage Rating Gate Open Circuited	1
				0.1		$T_C = +25^{\circ}C$	7
				0.5		$T_{\rm C} = +100^{\circ}{\rm C}$	7
Peak On-State Voltage	$V_{TM}$				Volts	$T_C$ = +25°C, $I_{TM}$ = 1 msec., Wide Pulse, Duty Cycle $\leq 2\%$	1
SC140		_		1.85		$I_{TM} = 9.2 \text{ A Peak}$	
SC141		_		1.83		$I_{TM} = 8.5 A Peak$	
SC142			_	1.75		I <sub>TM</sub> = 11.5 A Peak	
SC143			_	1.55		$I_{TM} = 11.5 A Peak$	
SC146		_	_	1.65		I <sub>TM</sub> = 14 A Peak	
SC147		_	_	1.50		I <sub>TM</sub> = 14 A Peak	
SC149				1.65		I <sub>TM</sub> = 17 A Peak	
SC151		_		1.52		I <sub>TM</sub> = 21 A Peak	
Critical Rate-of-Rise of Off-State Voltage (Higher values may cause device switching)	dv/dt				Volts/μsec	T <sub>C</sub> = +100°C, Rated V <sub>DRM</sub> Gate Open Circuited Exponential Voltage Waveform	1
SC140, SC141		30	100	_	]		
SC142, SC143		50	150	_			
SC146, SC147		100	150		]		
SC149		100	200		_		
SC151		100	250				
Critical Rate-of-Rise of Commutating Off-State Voltage (Commutating dv/dt)	dv/dt <sub>(c)</sub>	4	-	_	Volts/μsec	I <sub>T(RMS)</sub> = Rated Maximum Allowable RMS On-State Current, V <sub>DRM</sub> = Maximum Rated Peak Off-State Voltage, Gate Open Circuited.	1, 4
DC Gate Trigger	$I_{GT}$				mAdc	$V_D = 12 \text{ Vdc}$	2
Current						TRIGGER MODE RL TC	
				50		MT2+ Gate + 100 Ohms	
			_	50		MT2- Gate - 100 Ohms +25°C	C
			_	50		MT2+ Gate - 50 Ohms	
				80		MT2+ Gate + 50 Ohms	Į
			_	80		MT2- Gate - 50 Ohms -40°C	
				80		MT2+ Gate - 25 Ohms	
DC Gate Trigger	$V_{GT}$				Vdc	$V_D = 12 \text{ Vdc}$	2
Voltage						TRIGGER MODE RL TC	
				2.5		MT2+ Gate + 100 Ohms	
				2.5		MT2- Gate - 100 Ohms +25°	
	[			2.5		MT2+ Gate – 50 Ohms	
				3.5		MT2+ Gate + 50 Ohms	
				3.5		MT2- Gate - 50 Ohms -40°	
			_	3.5		MT2+ Gate – 25 Ohms	
DC Gate Non-Trigger	$V_{\mathrm{GD}}$	0.2	-	-	Vdc	TRIGGER MODE RL TC	2, 3
Voltage		1	1			MT2+ Gate +	
					1	MT2- Gate - 1000 +100	c
						MT2+ Gate – Ohms	
			1		1	MT2- Gate +	

TEST	CVMDOL	AALNI	TVO	MAY	LINUTO	TEST COMPLITIONS	DEE NOTE
<del></del>	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	REF. NOTE
DC Holding Current	I <sub>H</sub>		:		m <b>A</b> dc	Main Terminal Source Voltage = 24 Vdc Peak Initiating On-State Current = 0.5 A, 0.1 milliseconds to 10 milliseconds wide pulse, Gate Trigger Source = 7V, 20 Ohms.	1
			_	50		$T_C = +25^{\circ}C$	1
			_	100		$T_C = -40^{\circ}C$	<u> </u>
DC Latching Current	IL				mAdc	Main Terminal Source Voltage = 24 Vdc Gate Trigger Source = 15V, 100 Ohms, 50μsec pulse width, 5 μsec rise and fall times maximum  TRIGGER MODE  ΤC	2
			-	100		MT2 + Gate +	
				100		MT 2 - Gate - +25°C	
			-	200		MT2 + Gate -	
				200		MT2 + Gate +	
				200		MT 2 - Gate40°C	
				400		MT2 + Gate -	
Steady State Thermal Resistance	$R_{\theta JA}$			75	°C/Watt	Junction-to-Ambient	1, 5
Steady State Thermal Resistance	$R_{\theta JC}$				°C/Watt	Junction-to-Case This characteristic is useful as an	1, 6
SC140		-		3.1		acceptance test at an incoming in-	
SC141		·		3.0	]	spection station.	1
SC142				3.3			
SC143				3.2			(
SC146				2.2			
SC147				2.5			
SC149				2.0			1
SC151				2.0			
Apparent Thermal Resistance	R <sub>\theta JC(ac)</sub>		 		°C/Watt	Junction-to-Case This characteristic is useful in the	7
SC140				2.04		calculation of junction temperature rise above case temperature for AC	
SC141				2.22		current conduction.	
SC142				2.31	]		
SC143				1.97			
SC146	ļ			1.50			
SC147				1.69	}		
SC149	ļ			1.52	1	1	
SC151	·			1.10	i	<u></u>	<u>i</u>

## NOTES:

- 1. Characteristic values apply for either polarity of main terminal 2 referenced to main terminal 1.
- 2. Main terminal 1 is the reference terminal for main terminal 2 and gate terminal.
- With V<sub>D</sub> equal to maximum allowable off-state voltage.
- 4. Values for these test conditions are:

Device	Commutating di/dt	TC
SC140	3.5 A/msec	+80°C
SC141	3.2 A/msec	+80°C
SC142	4.3 A/msec	+75°C
SC143	4.3 A/msec	+80°C
SC146 / SC147	5.4 A/msec	+80°C
SC149	6.4 A/msec	+75°C
SC151	8.1 A/msec	+80°C

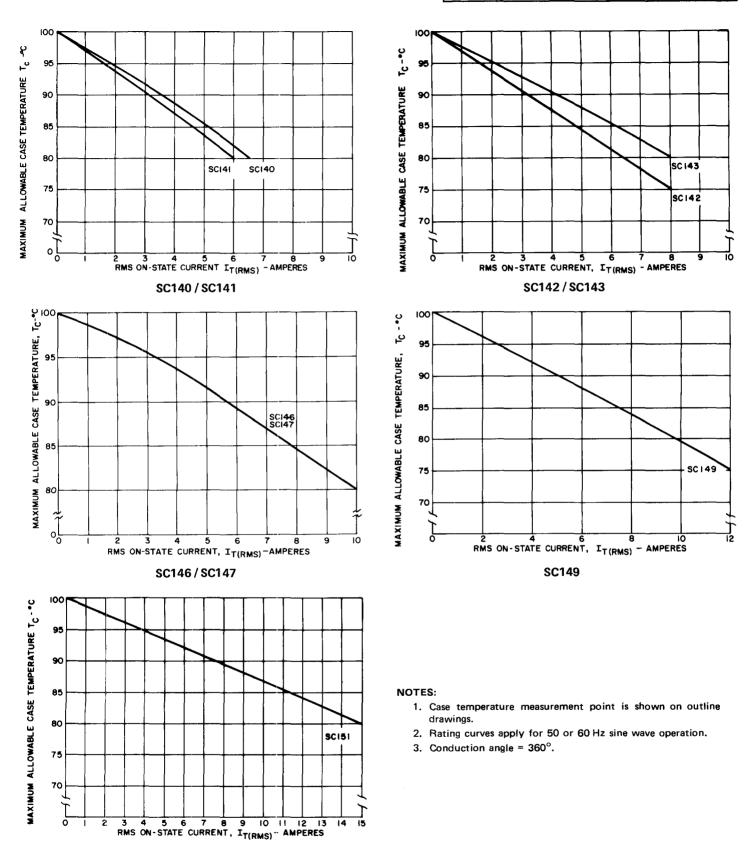
- 5. The junction-to-ambient value is under worst case conditions; i.e., with No. 22 copper wire used for electrical contact to the terminals and natural convection cooling.
- 6. Junction-to-case steady-state thermal resistance  $(R\theta_{JC})$  is tested in Junction-to-case steady-state thermal resistance  $(R_{\theta,C})$  is tested in accordance with EIA-NEMA Standard RS-397, Section 3.3.2, which states: "Thermal characteristics are to be measured with the device operating in only one direction." The values listed are the limiting value for either direction. For non-isolated devices, the MT2 lead temperature reference point is approximately equal to the case temperature reference point (see outline drawing).
- 7. Apparent thermal resistance applies for a 50 or 60 Hz full sine wave of current. It can be calculated with the following formula:

Apparent thermal resistance = 
$$\frac{T_{J(max)} - T_{C}}{P_{T(AV)}}$$

 $T_{J(max)}$  = maximum junction temperature  $T_{C}$  = case temperature where: T<sub>C</sub> = case temperature P<sub>T</sub>(AV) = average on-state power

See Reference Chart 12.

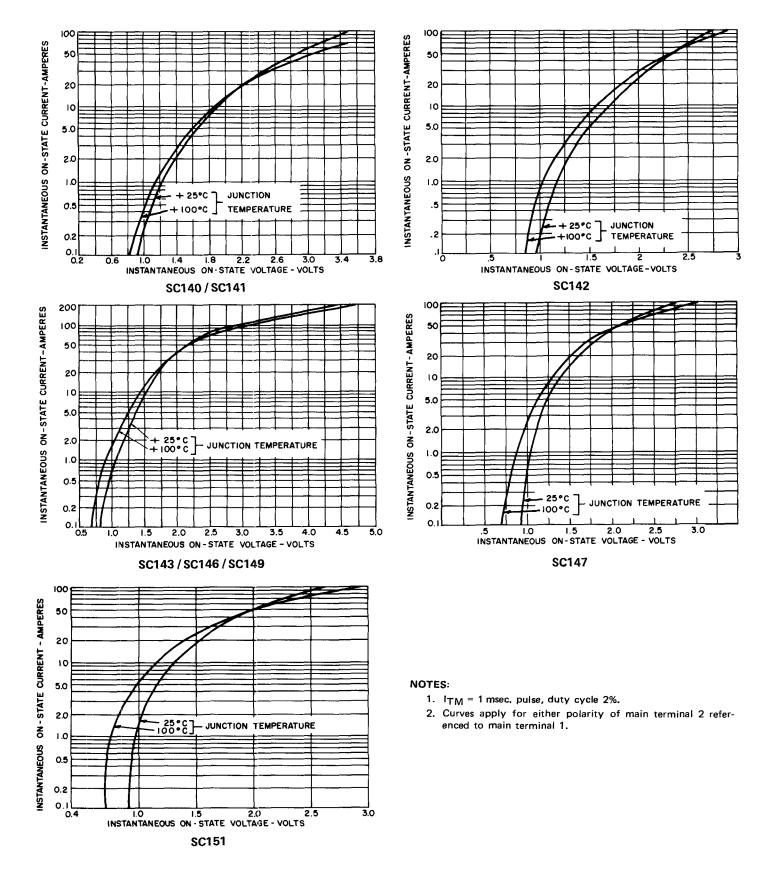
ISOLATED TAB	NON-ISOLATED TAB
SC140, 2, 7	SC141, 3, 6, 9, SC151



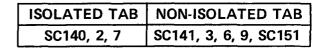
# 1. MAXIMUM CURRENT RATINGS

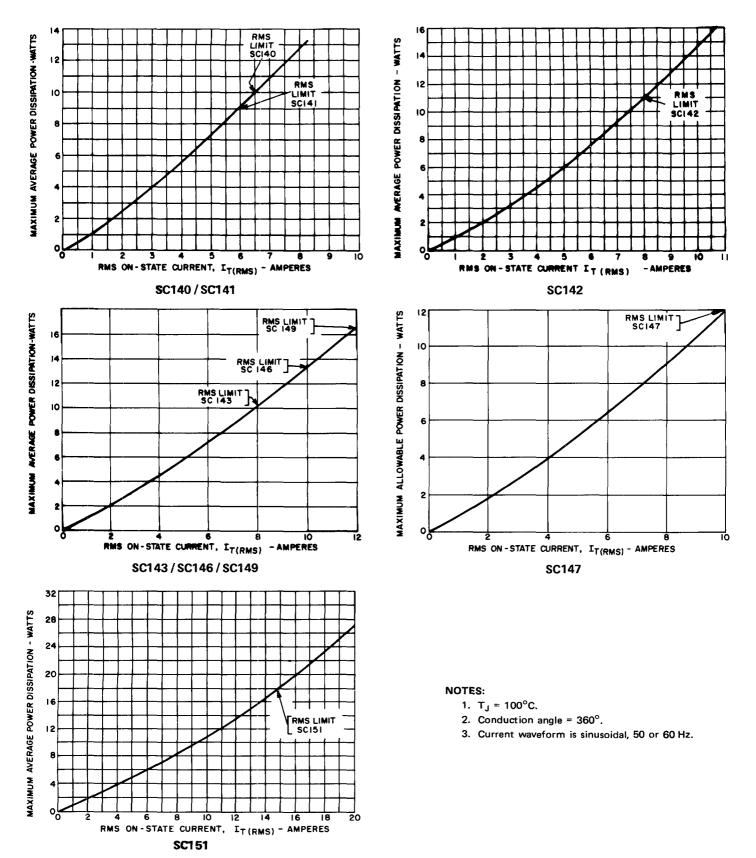
SC151

ISOLATED TAB	NON-ISOLATED TAB				
SC140, 2, 7	SC141, 3, 6, 9, SC151				

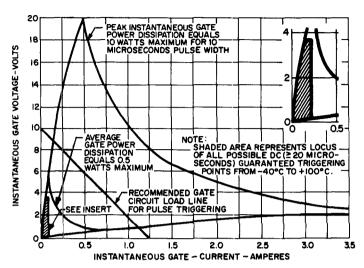


## 2. MAXIMUM ON-STATE CHARACTERISTICS

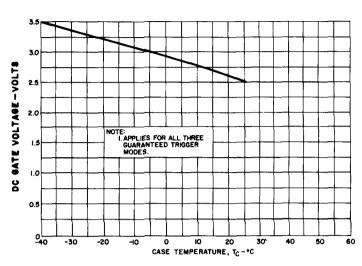




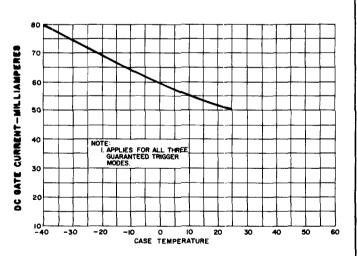
ISOLATED TAB	NON-ISOLATED TAB				
SC140, 2, 7	SC141, 3, 6, 9, SC151				



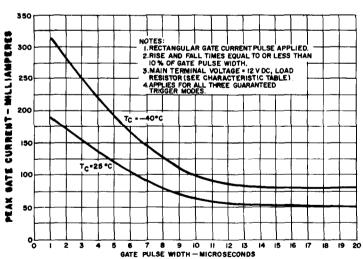
4. GATE CHARACTERISTICS AND RATINGS



5. MAXIMUM DC GATE VOLTAGE TO TRIGGER VERSUS CASE TEMPERATURE

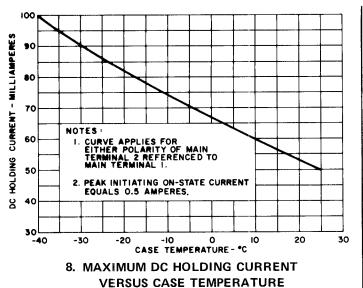


6. MAXIMUM DC GATE CURRENT TO TRIGGER VERSUS CASE TEMPERATURE



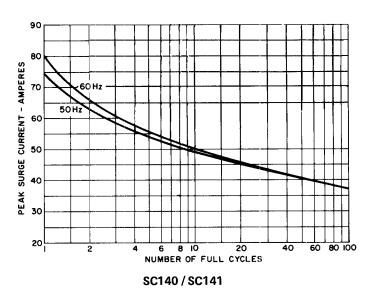
7. MAXIMUM GATE CURRENT TO TRIGGER VERSUS GATE PULSE WIDTH

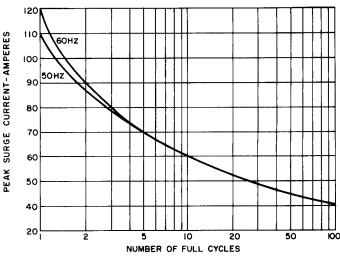
ISOLATED TAB	NON-ISOLATED TAB				
SC140, 2, 7	SC141, 3, 6, 9, SC151				



Đ.Đ COMMUTATING I. Tc = 80°C EXCEPT FOR Tc = 75°C 20 FOR SCI42 AND SCI49 2. FOR FULL WAVE CONDUCTION 10 di/dt(c) = IT(RMS)W RATED 707 WHERE: di/dt(c) IS IN AMPERES/MILLISECONDS TO DEVICE IT (RMS) IS IN AMPERES ω = 377 FOR 60Hz, 314 FOR 50Hz I RATED di/dt (C) NORMALIZED .2 TYPICAL COMMUTATING dy/dt-VOLTS/MICROSECOND

9. NORMALIZED DEVICE RATED COMMUTATING DI/DT VERSUS COMMUTATING DV/DT





SO HZ

4 6 8 10 20 NUMBER OF FULL CYCLES SC142/SC147

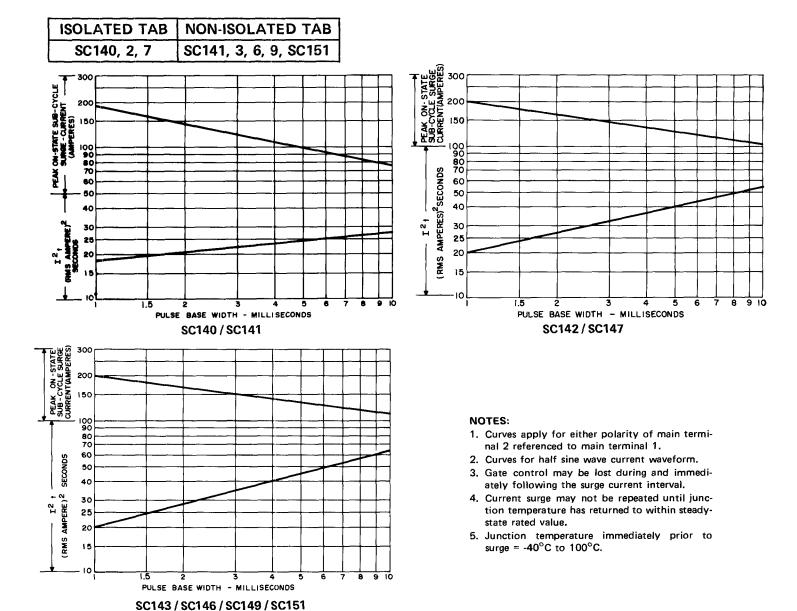
40

2

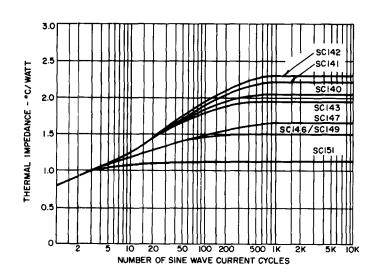
SC143/SC146/SC149/SC151

#### NOTES:

- Gate control may be lost during and immediately following the surge current interval.
- Current surge may not be repeated until junction temperature has returned to within steadystate rated value.
- 3. Junction temperature immediately prior to surge =  $40^{\circ}$ C to  $100^{\circ}$ C.



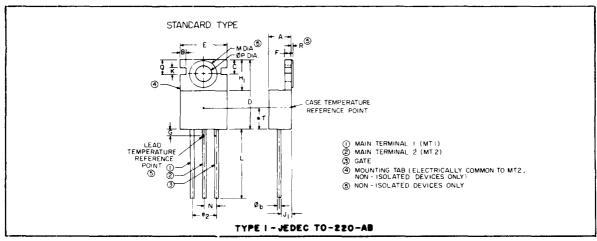
## 11. SUBCYCLE SURGE (NON-REPETITIVE) ON-STATE CURRENT AND I2t RATINGS



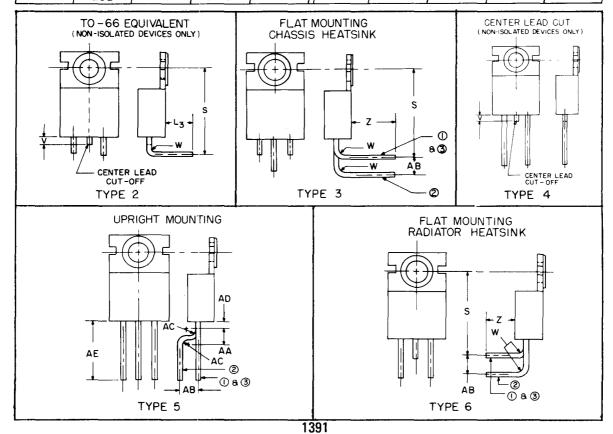
#### NOTES:

- Curve defines temperature rise of either junction above case temperature for equal amplitudes symmetrical sine wave current at 50 and 60 Hz.
- Curve considers junction temperature measured immediately after the final cycle of current.
- Gate will regain control if temperature is maintained below rated value and load current is reduced or maintained at RMS value.
- For more than 100 cycles of current the case temperature rise must be observed and used in calculating the total junction temperature.
- Junction temperature rise above case is defined as apparent transient thermal impedance times average conduction power dissipated during full cycle conduction.
- Apparent steady-state value is not the same as JEDEC value listed as steadystate in characteristics table.

ISOLATED TAB NON-ISOLATED TAB SC140, 2, 7 SC141, 3, 6, 9, SC151



CYMBO	INC	HES	METRI	CMM	CYMBO	INC	CHES	METE	RIC MM
SYMBOL	MIN	MAX	MIN	MAX	SYMBOL	MIN	MAX	MIN	MAX
Α	. 160	. 190	4.06	4.83	N	.095	.105	2.41	2.67
В	.054	TYP.	1.37	TYP.	ØР	.141	.145	3.58	3.68
Øb	.029	.035	.73	.89	Q	.118	REF.	3.00	REF.
С	.110	.120	2.79	3.05	R	.0015	.004	_	.10
D	.560	.650	14.23	16.51	S	.570	.590	14.47	14.99
E	.390	.420	9.90	10.67	T		.220		5.59
e <sub>2</sub>	.190	.210	4.82	5.33	V	.040	.070	1.01	1.78
F	.040	.055	1.01	1.39	w	.020	.030	.50	.76
G	_	.065	_	1.65	Z	.172	.202	4.36	5.13
H <sub>I</sub>	.240	.260	6.09	6.60	AA	.087	.097	2.20	2.46
JI	.085	.115	2.15	2.92	AB	.120	.130	3.04	3.30
К	.054	REF.	1.37	REF.	AC	.025	.035	.63	.89
L	.500	_	12.70		AD	.045	.055	1.14	1.40
Lg	.360		9.14		AE	.353	.433	8.96	11.00
M	.232	.236	5.89	5.99					



ISOLATED TAB	NON-ISOLATED TAB
SC140, 2, 7	SC141, 3, 6, 9, SC151

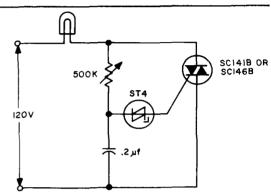
# POWER PAC TRIAC PART NUMBER DESIGNATION

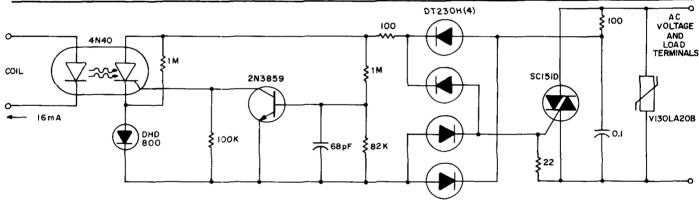
	SC1	40	B 2			
POWER PAC TRIAC			[	LEAD FOR	VING CONFI	<u>GURATIONS</u>
CURRENT RATING & ISOLATION				<b>VOLTAGE RATING</b>		
40 = 6.5 A RMS Isolated				B = 200  Volts	None = Star	ndard Type 1
41 = 6 A RMS Non-Isolated				D = 400 Volts	2 =	Type 2
42 = 8 A RMS Isolated				E = 500 Volts	3 =	Type 3
43 = 8 A RMS Non-Isolated				M = 600 Volts	4 =	Type 4
46 = 10 A RMS Non-Isolated					5 =	Type 5
47 = 10 A RMS Isolated					6 =	Type 6
49 = 12 A RMS Non-Isolated					NOTE: See	Outline Drawing.
51 = 15 A RMS Non-Isolated					.,0.2.	

# TYPICAL CIRCUITS

Triacs are especially useful in AC lamp dimming because of their ability to conduct in both directions.

The circuit shown here incorporates General Electric's ST4 asymmetrical AC trigger integrated circuit. This device greatly reduces the snap-on effects that are present in symmetrical trigger circuits and minimizes control circuit hysteresis. This performance is possible with a single RC time constant, whereas a symmetrical circuit of comparable performance would require at least three additional passive components.





The SC151D, in combination with an optically-isolated SCR (4N40), allows this highly transient immune, TTL compatible, zero voltage switching design for a normally open 15 ampere solid-state relay. Zero voltage crossing is sensed via the base emitter diode drop of the 2N3859 which then allows the 4N40 SCR portion to be triggered and apply gate signal to the SC151 triac. The transient immunity is designed in through use of the GE-MOV®, the snubber network and the choice of 400 volt semiconductors.

OTHER TR	IIAC, TRIGGE	R AND APPLICATION INFORM	IAVA NOITAN	LABLE FROM GENERAL ELECTRIC	
PUBLICATION NUMBER	TRIAC SPECIFICATION SHEETS		PUBLICATION NUMBER	APPLICATION NOTES	
175.13	SC136		200.35	Using the Triac for Control of AC Power	
175.34	Hermetic Triacs		200.53	Solid State Incandescent Lighting Controls	
TRIGGER SPECIFICATION SHEETS		201.12	500 Watt AC Line Voltage and Pow Regulator		
175.30	ST2	(Diac)	201.19	RF Filter Considerations for Triac & SCR	
175.32	ST4	(Asymmetrical AC Trigger)	201.19	Circuits	
65.32	2N4992	(Silicon Bilateral Switch)	201.24	Thyristor Selection for Incandescent Lamp	
RELIABILITY REPORT				Loads	
95.29 Glassivated Triac Reliability Report		200.55	Thermal Mounting Considerations for Plastic Power Semiconductor Packages		