signetics

J-K MASTER-SLAVE FLIP-FLOP

S54H72
N74H72

S54H72–A,F,W • N74H72–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state

TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

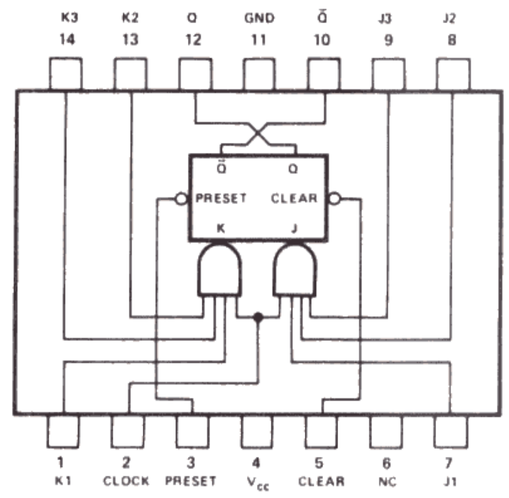
NOTES:

1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse
4. t_{n+1} = bit time after clock pulse.

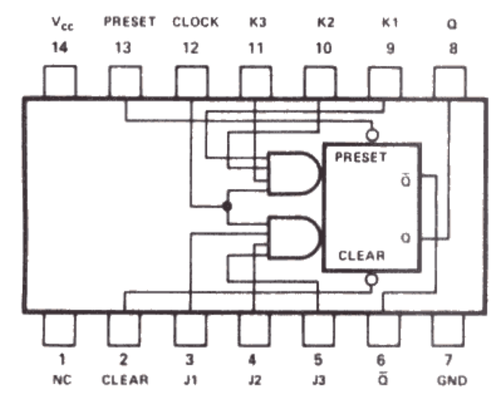
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

PIN CONFIGURATIONS

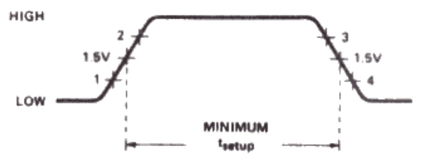
W PACKAGE



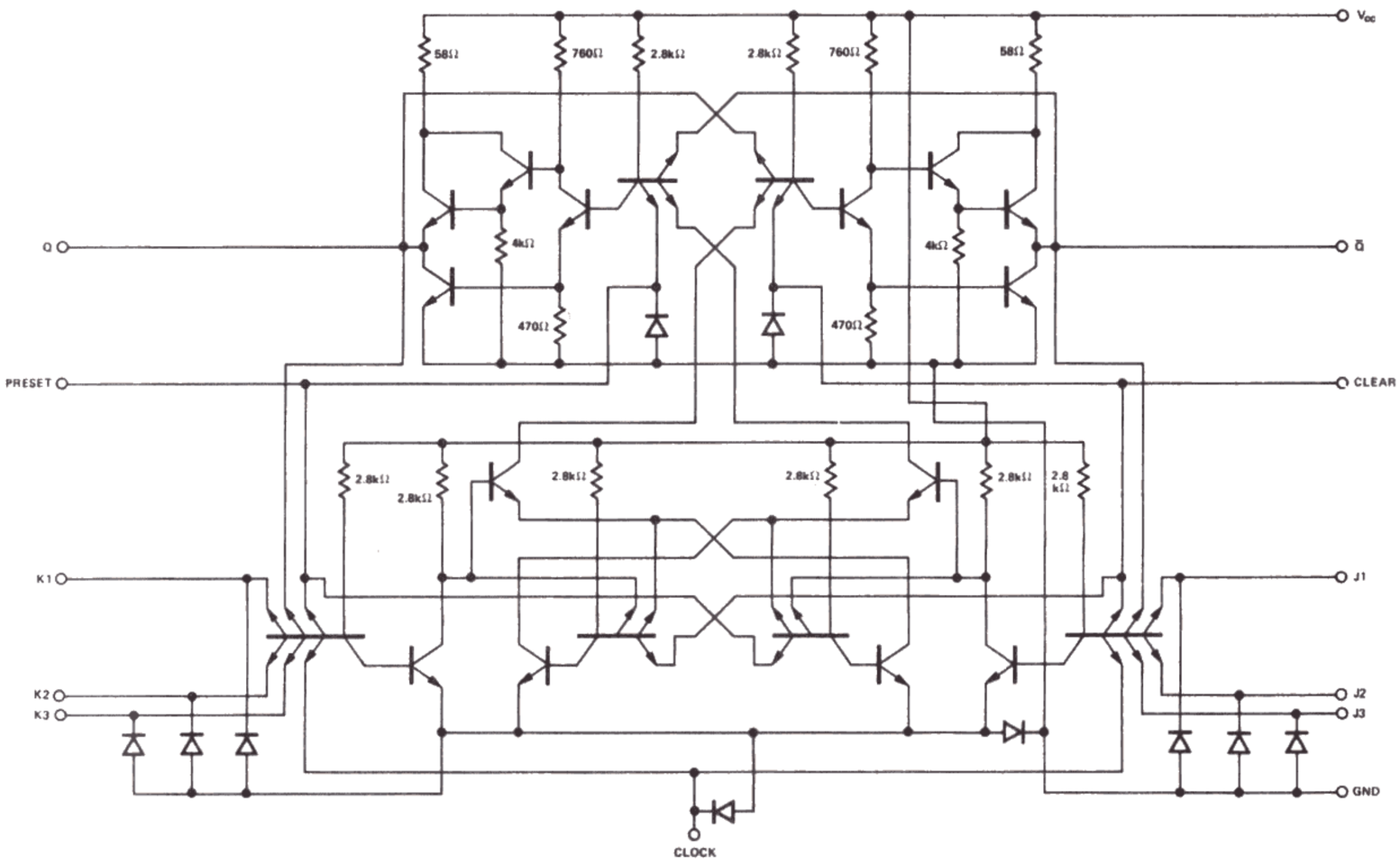
A,F PACKAGE



CLOCK WAVEFORM



SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

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RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H72 Circuits		4.5	5	5.5	V
N74H72 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H72 Circuits	-55	25	125	°C
	N74H72 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See above)		$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

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ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,			16	25	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

54/7400 PRODUCT INFORMATION

GENERAL DESCRIPTION

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7V
Input Voltage, V_{in} (See Note 1	5.5V
Interemitter Voltage (See Note 2)	5.5V
Resistor Node Voltage, 54121, 74121 (See Note 1)	-5.5V to 7V
Operating Free-Air Temperature Range:	
Series 54 Circuits	-55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests 1 output at a time.

Series 54/74 Logic Family
The 54/74XX logic family is medium speed TTL, and high speed TTL integrated circuits. The family includes a multiple number of functions in a variety of packages. The 54XX devices are characterized for the full military temperature range of -55°C to +125°C. The 74XX devices are characterized for the limited temperature range of 0°C to +70°C.

INPUT CLAMPING DIODES

Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if -12mA of current is drawn.

DESIGN CONSIDERATIONS

Logic Definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:
LOW VOLTAGE = LOGICAL "0"
HIGH VOLTAGE = LOGICAL "1"

Unused Inputs
For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4V but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package load, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to a supply voltage. Preferably, this voltage should be between 2.4V and 5.5V.
b. Connect unused inputs to a used input if maximum fanout of the driving output will not be exceeded. Each input presents a full load in the logical "1" state to the driving output.

Input-Current Requirements
Input-current requirements reflect worst-case V_{CC} and temperature condition. Currents into the input terminals are specified as positive values.

54/74 Logic
Each input of the multiple-emitter input transistor that utilizes a 4 KΩ resistor requires no more than -1.6 mA flow out of the input at a logical "0" voltage level; therefore, one load (N = 1) for 54/74 logic is -1.6 mA maximum. Each input requires current into the input at a logical "1" voltage level. This current is 40μA maximum for each emitter input.

Fanout Capability
Fanout reflects the ability of an output to sink current from a number of loads (N) at a logical "0" voltage level and to supply current at a logical "1" voltage level. Each standard 54/74 output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate (54/7440) is capable of sinking current or supplying current to 30 loads (N = 30).

ELECTRICAL CHARACTERISTICS

These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted, as shown in Section 2 of the handbook.

NOTE
Any product available in an A or B package can also be supplied in the F cerdip package.

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S54

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TEMPERATURE RANGE*

S54 = -55°C to +125°C (Military Range)

N74 = 0°C to +70°C (Industrial Range)

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PART IDENTIFICATION

Must contain two to four characters.

Examples:
00
H20
107

W

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PACKAGE*

"A" = 14-pin dual in-line silicone package (TO-116)
"B" = 16-pin dual in-line silicone package
"F" = 14-16 pin cerdip
"N" = 24-lead dual in-line silicone package
"Q" = 24-pin ceramic flat-pak
"W" = 14-16 pin flat cerpac
"F" = 24-pin ceramic dual in-line package

*Availability of a circuit device in a particular package and temperature range is indicated on the appropriate device. Electrical Characteristics Data Sheet is shown in Section 2 of this handbook.

Manufacturer reserves the right to make design and process changes and improvements.